

DR11B

DIAGNOSTIC
MD-11-DZDRB-D

EP-DZDRB-D-DL-A
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FICHE 1 OF 1

NOV 1976
digital
MADE IN USA

The microfiche card contains a grid of frames on the left side, which are organized into columns and rows. Each frame contains technical data, likely related to a diagnostic procedure for an MD-11 aircraft. The data is presented in a structured format, possibly as a table or a list of parameters. The frames are arranged in a grid that is approximately 10 columns wide and 15 rows high. The text within the frames is small and difficult to read, but it appears to be organized into sections or tables. The right side of the card is mostly blank, with some faint markings and a small vertical strip of text near the bottom right corner.

1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 34 35 36 37 38 39 40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63 64 65 66 67 68 69 70 71 72 73 74 75 76 77 78 79 80 81 82 83 84 85 86 87 88 89 90 91 92 93 94 95 96 97 98 99 100

1. ABSTRACT

1.1 THIS IS A LOGIC TEST OF THE "NPR GENERAL INTERFACE" -DR118.
THERE IS A SPECIAL MAINTENANCE FEATURE THAT ALLOWS TESTING
OF YPRS WITHOUT A CUSTOMERS DEVICE ATTACHED.
1.2 THERE IS A SECOND TEST INCLUDED FOR EXERCISING THE DR118
INTERPROCESSOR LINK. THE DR118 TEST SHOULD BE RUN IN
IN EACH COMPUTER BEFORE TESTING THE DR118.

2. REQUIREMENTS

2.1 EQUIPMENT

2.1.1 FOR THE DR118

PDP-11 STANDARD COMPUTER

DR118

NOTE: WITH OR WITHOUT HARDWARE SWITCH REGISTER

2.1.2 FOR THE DR118

2 PDP-11 STANDARD COMPUTERS

1 DR118 CONSISTING OF 2 M7229 MODULES AND 2
BC09R CABLES.

NOTE: WITH OR WITHOUT HARDWARE SWITCH REGISTER

2.2 STORAGE

2.2.1 PROGRAM STORAGE - THE ROUTINE USES MEMORY
FROM 0 TO 14000.

3. LOADING PROCEDURE

3.1 METHOD

PROCEDURE FOR NORMAL BINARY TAPES SHOULD BE FOLLOWED.

4. DR118 STARTING PROCEDURE

4.1 CONTROL SWITCH SETTING

STARTING AT SA 200 ALL SWITCHES SHOULD BE DOWN OR ZERO.

4.2 STARTING ADDRESS OR ADDRESSES

(A) 200 = TEST OF LOGIC USING MAINTENANCE FEATURE M969 IN 004,004

4.3 PROGRAM AND OR OPERATOR ACTION

LOAD PROGRAM INTO MEMORY.
LOAD STARTING ADDRESS
PRESS START.
THE PROGRAM WILL LOOP, BELL WILL RING ONCE
PER PASS OF THE PROGRAM.

NOTE: IF SOFTWARE SWITCH REGISTER IS SELECTED THEN THE
FOLLOWING WILL BE PRINTED:

SWR= XXXXX NEW=
(REFER TO SECTION 5.1 FOR OPERATOR OPTIONS)

5. DR11B OPERATING PROCEDURE

5.1 OPERATIONAL SWITCH SETTINGS

5.1.1 AT SA 200 ... THE INSTRUCTION AND LOGIC TEST.
WITH ALL SWITCHES DOWN THE PROGRAM WILL PRINT
OUT ON ERRORS AND CONTINUE IN TEST. (BELL
WILL RING AT COMPLETION OF A PASS)

5.1.2 SWITCH SETTINGS ARE

SW15 = 1 OR LP ... HALT ON ERROR
SW14 = 1 OR UP ... SCOPE LOOP
SW13 = 1 OR UP ... INHIBIT PRINTOUT
SW12 = 1 OR LP ... INHIBIT TRACE TRAP
SW11 = 1 OR UP ... INHIBIT ITERATIONS

5.1.3

IF THE DIAGNOSTIC IS RUN ON A CPU WITHOUT A SWITCH
REGISTER THEN A SOFTWARE SWITCH REGISTER IS USED WHICH ALLOWS
THE USER THE SAME SWITCH OPTIONS AS THE HARDWARE SWITCH REGISTER.
IF THE HARDWARE SWITCH REGISTER DOES NOT EXIST OR IF ONE DOES
AND IT CONTAINS ALL ONES (177777) THEN THE SOFTWARE SWITCH
REGISTER (LOC. 176) IS USED.

CONTROL:

THIS PROGRAM ALSO SUPPORTS THE DYNAMIC LOADING OF THE SOFTWARE SWITCH
REGISTER (LOC. 176) FROM THE TTY. THIS CAN BE ACCOMPLISHED BY
DOING THE FOLLOWING:

- 1) TYPE CONTROL G (1G): THIS WILL ALLOW THE TTY TO ENTER DATA INTO
LOC. 176 AT SELECTED POINTS WITHIN THE PROGRAM.
- 2) THE MACHINE WILL THEN TYPE: SWR=XXXXXXXXNEW= (XXXXXX IS THE OCTAL CONTENTS
OF THE SOFTWARE SWITCH REGISTER.)
- 3) AFTER THE "NEW=" HAS BEEN TYPED THE OPERATOR CAN DO ONE
OF THE FOLLOWING AT THE TTY:
 - a) TYPE A NUMBER TO BE LOADED INTO LOC. 176 FOLLOWED BY A CR:
(ONLY NUMBERS BETWEEN 0-7 WILL BE ACCEPTED AND ONLY 6 NUMBERS
WILL BE ALLOWED)

IF A (CR) IS THE FIRST KEY DEPRESSED THE SOFTWARE SWITCH REGISTER CONTENTS WILL NOT BE CHANGED.

B) IF A CONTROL U (IU) IS DEPRESSED THEN THE PROGRAM WILL SEND YOU BACK TO STEP 2.

5.2. SUBROUTINE ABSTRACTS

BEGIN SA 200

5.2.1 SCOPE

THIS SUBROUTINE CALL IS PLACED BETWEEN EACH SUBTEST IN THE INSTRUCTION SECTION. IT RECORDS THE STARTING ADDRESS OF EACH SUB-TEST AS IT IS BEING ENTERED. IF A SCOPE LOOP IS REQUESTED, IT WILL JUMP TO THE START OF THE SUBTEST THAT THE SCOPE LOOP IS REQUESTED FOR. IF SCOPE LOOP IS NOT REQUESTED, THERE WILL BE EITHER A FIXED OR RANDOM NUMBER OF ITERATIONS ON THAT SUBTEST BEFORE THE NEXT SUBTEST IS ENTERED. SWITCH 11 ON A 1 INHIBITS ITERATION OF SUBTESTS.
NOTE: SUPPORTS IG ROUTINE FOR DYNAMIC LOADING OF SOFTWARE SWITCH REGISTER

5.2.2 HALT

IS A ROUTINE THAT PRINTS-OUT AN ADDRESS THAT TAGS THE FAILING SUBTEST, THE CP STATUS REGISTER AND THE DR11B STATUS REGISTER AT THE TIME OF FAILURE.
NOTE: SUPPORTS IG ROUTINE FOR DYNAMIC LOADING OF SOFTWARE SWITCH REGISTER

5.2.3 LODBUF

THE INBUF BUFFER IS LOADED WITH AN INCREMENTING PATTERN (0,1,2,3,...) BEGINNING AT THE STARTING ADDRESS OF INBUF. THE NUMBER OF WORDS LOADED IS DETERMINED BY THE CONTENTS OF BUFLen.

5.2.4 CHKBUFF

THE CHKBUFF BUFFER IS LOADED WITH A MODIFIED INCREMENTING PATTERN (0,0,2,2,4,4,6,6,...) BEGINNING AT THE STARTING ADDRESS OF CHKBUFF. THE NUMBER OF WORDS LOADED IS DETERMINED BY THE CONTENTS OF BUFLen. THIS BUFFER IS LOADED ONLY FOR TESTS WHICH USE THE MAINTENANCE MODE OF THE DR11-B WHICH HAS A SPECIAL ALTERNATING DATA-DATA SEQUENCE OF OPERATION.

5.2.5 INTA

THE IE BIT IS CLEARED IN THE DRST THEN THE DRST IS CHECKED FOR THE ABSENCE OF AN ERROR AND THE PRESENCE OF READY. THE DRWC IS CHECKED TO SEE THAT IT IS EQUAL TO ZERO. THE CORRECT CONTENTS

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OF THE DRBA ARE CALCULATED AND CHECKED. THERE IS A JSR TO THE NORMAL SUB-ROUTINE BEFORE THIS ROUTINE IS EXITED. THE PROGRAM WILL HALT IF ERROR IS SET, READY IS CLEAR, OR READY AND ERROR ARE CLEAR.

5.2.6 DATCHK

THIS ROUTINE IS ENTERED. CHECK INBUF AFTER A MAINTENANCE MODE OPERATION. THE CONTENTS OF INBUF AND THE CONTENTS OF CHKBUF ARE CHECKED TO SEE THAT THEY ARE THE SAME. THE NUMBER OF COMPARISONS MADE IS DETERMINED BY THE CONTENTS OF BUFLN.

5.2.7 NORMAL

THE ROUTINE IS ENTERED FROM INTA AND FROM SOME TESTS WHICH DON'T USE INTA. THE NUMBER OF THE DRINV+2 IS PUT INTO DRINV AND THE DRYS IS CLEARED. IF THE DR11-B INTERRUPTS UNDER THESE CONDITIONS THE PDP-11 WILL HALT AT DRYS. THE PROCESSOR STATUS WORD IS RESTORED TO LEVEL 7 AND THE ROUTINE IS EXITED.

5.2.8 DATOCK

AFTER A STRING OF DATO'S HAS BEEN COMPLETED THIS ROUTINE CHECKS THAT THE CORRECT DATA PATTERN (52525) WAS TRANSFERRED TO INBUF. THE NUMBER OF COMPARISONS MADE IS DETERMINED BY THE CONTENTS OF BUFLN. AN ADDITIONAL CHECK IS MADE ON BUFLN+2 TO INSURE THAT TOO MANY WORDS WEREN'T TRANSFERRED.

5.2.9 ERRCHK

THIS ROUTINE CLEARS IE AND HALTS IF ERROR IS SET.

5.2.10 TRAPCATCHER

THIS IS A SERIES OF INSTRUCTIONS STARTING AT LOCATION 0 DESIGNED TO DETECT AND ISOLATE UNEXPECTED TRAPS AND INTERRUPTS TO THE TRAP AND INTERRUPT VECTOR AREA OF MEMORY.

EACH VECTOR ENTRANCE ADDRESS IS LOADED WITH THE ADDRESS OF THE NEXT LOCATION. THE NEXT LOCATION IS LOADED WITH A HALT (000000). THUS AN ILLEGAL TRAP OR INTERRUPT WILL CAUSE A HALT AT THE TRAP LOCATION PLUS TWO.

IF A HALT OCCURS IN THE TRAP OR INTERRUPT AREA, EXAMINE REGISTER SIX, IT WILL CONTAIN THE CURRENT STACK ADDRESS. THE CONTENTS OF THE CURRENT STACK ADDRESS IS THE VALUE OF THE LOCATION COUNTER WHEN THE TRAP OR INTERRUPT OCCURRED.

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5.3 PROGRAM AND/OR OPERATOR ACTION

5.3.1 LOADING AND STARTING AT 200 ITH ALL SWITCHES DOWN IS THE INSTRUCTION AND LOGIC TEST. IF AN ERROR IS DETECTED HERE, THERE WILL BE A PRINTOUT. WHEN AN ERROR IS DETECTED AND IT IS NECESSARY TO SCOPE ON IT, PLACE SW15 UP TO HALT ON ERROR, THEN SW14 UP TO LOOP ON ERROR, THEN SW13 UP TO DELETE PRINTOUTS.

6. DR11B ERRORS

6.1 ERROR PRINTOUT

THE PC OF THE FAILING TEST AND THE CP STATUS WILL BE PRINTED.

6.2 ERROR RECOVERY

DEPRESS CONTINUE TO RESTART SECTION

7. DR11B RESTRICTIONS

7.1 STARTING RESTRICTION

NONE

7.2 OPERATIONAL RESTRICTION

M968 MUST BE IN SLOTS C04/D04 - FOR DIAGNOSTIC TESTING SHOULD BE IN A02/B02 FOR NORMAL USER OPERATION.

8. MISCELLANEOUS

8.1 EXECUTION TIME

ABOUT 2 MINUTES

9. PROGRAM DESCRIPTION

THE FOLLOWING IS A GENERAL LIST OF FUNCTIONS TESTED.

- CAN ALL REG BE ADDRESSED WITHOUT ERROR
- RESET CLEAR DRWC
- RESET CLEAR DRBA
- CAN ALL DRWC BITS BE SET
- CAN 15-i IN DRBA BE SET
- FNCT1 SET & CLEARED
- FNCT2 SET & CLEARED
- FNC-3 SET & CLEARED
- XBA16 SET & CLEARED
- XBA17 SET & CLEARED
- IE SET & CLEARED
- CYCLE SET & CLEARED

מחלקת תחזוקה
מפעל תעשיית הנפט
תל אביב-יפו
רחוב הנפט 1
טל. 03-5222222

MAINT SET & CLEARED
 ALL DRST R/W BITS CAN BE SET & CLEARED
 ALL DRST R/W SET, RESET TO 0. RDY IS SET, NEX IS
 CLEARED, GO IS 0
 DRWC HOLD ALT. 0'S & 1'S AND ALT. 1'S & 0'S
 DRBA HOLD ALT. 0'S & 1'S AND ALT. 1'S & 0'S
 INC PATTERN TO WRAP-AROUND IN DRWC
 INC PATTERN TO WRAP-AROUND IN DRBA
 NO INT. AT LEVEL 7
 NO INT. AT LEVEL 6
 NO INT. AT LEVEL 5
 DOES INT. AT LEVEL 4
 NO MAINTBRD A02/B02
 MAINTBRD C04/D04
 FNCT BITS CONTROL DSTAT BITS
 RESET C'S DRDB
 ALL DRDB BITS CAN BE SET
 DRDB HOLD ALT. 1'S & 0'S AND ALT. 0'S & 1'S
 INC TO WRAP-AROUND IN DRDB
 RESET SETS ONLY RDY IN DRST
 BA00 READS AS 0
 1 DAT1 NPR
 1 DAT0 NPR
 BA0F FORCES ERROR & IS CLEARED BY CLEARING DRBA OR RESET
 30 CLEARS RDY
 DAT0 TO DIODE MEM CAUSES NEX
 DO WITHOUT CLEARING PREVIOUS ERROR CAUSES ANOTHER INT.
 10 DAT1'S (BURST)
 10 DAT0'S (BURST)
 200 DAT1'S (BURST)
 200 DAT0'S (BURST)
 200 DAT1'S (NON-BURST)
 200 DAT0'S (NON-BURST)
 FUNCT BITS INC WITH MAINT MODE XFERS
 10 MAINT MODE XFERS
 200 MAINT MODE XFERS

10. LISTING

11. FLOW CHART(S)

12. DA11B STARTING PROCEDURE

- 12.1 THERE ARE TWO STARTING LOCATIONS: ONE FOR THE
COMPLTER THAT WILL BE THE SLAVE AND ANOTHER
FOR THE COMPUTER THAT WILL BE THE MASTER.
- 12.2 SLAVE COMPUTER, LOAD ADDRESS 1002 WITH THE HALT KEY
DOWN AND PRESS START.
- 12.3 MASTER COMPUTER, LOAD ADDRESS 1000 WITH THE HALT KEY
DOWN AND PRESS START.

12.4 SLAVE COMPUTER. PUT THE HALT KEY UP AND PRESS CONTINUE.

12.5 MASTER COMPUTER. PUT THE HALT KEY UP AND PRESS CONTINUE.

13. DA119 OPERATING PROCEDURE

13.1 THE PROGRAM WILL LOOP AFTER STARTING AND PRINT OUT ANY ERRORS. THE PROGRAM WILL HALT AFTER NON RECOVERABLE ERRORS.

13.2 THE MAINT MODULE MUST BE IN A02/B02 AND THE THE DA11B MUST BE IN C04/D04 .

14. DA11B PROGRAM DESCRIPTION

14.1 THE SLAVE COMPUTER STARTS BY ENTERING A BACKGROUND TO WAIT FOR AN INTERRUPT WITH THE INTERRUPT ENABLED. THE FIRST INTERRUPT THAT COMES SHOULD BE THE READY INTERRUPT SET UP WHEN THE MASTER HIT THE START KEY. THE INTERRUPT CAUSES THE SLAVE TO ENTER THE INTERRUPT SERVICE ROUTINE.

14.2 THE INTERRUPT SERVICE ROUTINE DETERMINS WHAT INTERRUPT CAME UP AND IF IT SHOULD HAVE COME UP. IF THE INTERRUPT WAS THE ONE EXPECTED THAN THE THAN THE PROGRAM GOES TO THE TO THE PROPER JOB ROUTINE, SJOBXX FOR SLAVE SERVICE AND JOBXX FOR THE MASTER ROUTINE.

14.3 THE NEXT THING THAT SHOULD HAPPEN IS THE MASTER SHOULD ISSUE AN INTERRUPT TO THE SLAVE THIS IS A SIGNAL FOR THE SLAVE TO ACCEPT THE WORD COUNT, OFFSET AND TWO CHECK SUM WORDS. THE SLAVE ACCEPTS A WORD AT A TIME FROM THE DATA BUFFER EACH TIME THE MASTER TOGGLES FUNCTION BIT 3. EACH TIME IT READS A WORD THE SLAVE SENDS THE WORD BACK TO THE MASTER FOR VERIFICATION.

14.4 AFTER THE SLAVE HAS RECIEVED ALL THE PARAMETERS IT SETS ITS DIRECTION BIT TO THE OPPOSIT DIRECTION AS THE MASTER AND STARTS THE NPR TRANSFER.

14.5 THE MASTER SETS UP THE TYPE OF TRANSFERS AND CHECKS THE DATA WHEN IT COMES BACK FROM THE SLAVE.

15. DA117 ERRORS

15.1 THE PC OF THE FAILING TEST, THE CP STATUS AND THE DA11B STATUS REGISTER WILL BE PRINTED AFTER AN ERROR.

15.2 THERE IS NO ERROR RECOVERY FOR THE DA11B TEST BECALSE THE OTHER COMPUTER WILL GET OUT OF SYNC WHEN AN ERROR OCCURS.

0000-1000 1111-2222 3333-4444 5555-6666 7777-8888 9999-0000 1111-2222 3333-4444 5555-6666 7777-8888 9999-0000

4432
4433
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000001
160000

000240
104400
104000
000001
000002
000004
000010
000020
000040
000100
000200
000400
001000
002000
004000
010000
020000
040000
100000

000004

000000
000030
000030 011072
000032 000340

```

      .ABS
      .MCALL .HEADER,STARS
:*****
:*****
:TITLE MAINDEC-11-DZDRB-D
:*COPYRIGHT (C) 1971,1976
:*DIGITAL EQUIPMENT CORP.
:*MAYNARD, MASS. 01754
:*
:*PROGRAM BY POMFRET,JONES.CONDON
:*
:*THIS PROGRAM WAS ASSEMBLED USING THE PDP-11 MAINDEC SYSMAC
:*PACKAGE (MAINDEC-11-DZQAC-C2), SEPT 14, 1976.
:*
$TN=1
$SWR=160000 ;:HALT ON ERROR, LOOP ON TEST, INHIBIT ERROR TYP0UT
:*****
:      REVISED BY ALAN BOSTICK JUNE 1976
:      MODIFIED FOR SOFTWARE SWITCH REGISTER
:      INCLUDING DYNAMIC LOADING OF SWR
:*****
:*****
      NOP=000240
      SCOPE=TRAP
      HLT=EMT
      BIT0=000001
      BIT1=000002
      BIT2=000004
      BIT3=000010
      BIT4=000020
      BIT5=000040
      BIT6=000100
      BIT7=000200
      BIT8=000400
      BIT9=001000
      BIT10=002000
      BIT11=004000
      BIT12=010000
      BIT13=020000
      BIT14=040000
      BIT15=100000

      BUSERR=000004

;LOAD TRAP CATCHER INTO 0 THRU 777.

      .=0
      .=30
      PRINT
      340

```

```

4.90 000034 000034
4.91 000036 011650
4.92 000036 000340
4.93 000176 000176
4.94 000176 000000
4.95 000200 000200
4.96 000200 012706 013566
4.97 000204 005077 000604
4.98 000210 005002
4.99 000212 012702 012433
000216 004767 012240
000222 012702 012403
000226 004767 012230
000232 000167 000634
001000 001000

```

```

.=34
SCOPEC
340
.=176
SWREG: 0
.=200
MOV #BUFF,%6 ;SET UP STACK LIMIT
CLR @PSW
CLR %2
MOV #SHEAD,%2
JSR %7,TTOUT
MOV #SMAIN,%2
JSR %7,TTOUT
JMP SUSWR
.=1000

```

```

:*****
: START OF BACK-TO-BACK DR11-B
:*****

```

```

001000 000402
001002 000167 006276
001006 000167 006212
001012 177570
001014 177776
001016 172410
001020 172412
001022 172414
001024 172416
001026 000126
001030 000240
001032 000124
001034 052525
001036 173000
001040 013570
001042 014572
001044 000000
001046 000000
001050 000000
001052 000000
001054 000000
001056 177560
001060 177562
001062 177564
001064 177566
001066 000000
001070 000000
001072 013746 000006
001076 013746 000004
001102 012737 001122 000004
001110 022777 177777 177574
001116 001402
001120 000404

```

```

MSTART: BR MSX ;MASTER START
SSTART: JMP SSI ;SLAVE START
MSX: JMP MSI
SR: 177570
PSW: 177776
DRWC: 172410
CRBA: 172412
DRST: 172414
DRDB: 172416
DRVS: 126
DRINL: 240
DRINV: 124
NPR1: 52525
DIOMEM: 173000
INBUF: XINBUF
CHKBUF: XCHKBU
BUFLN: HALT
LENCHK: HALT
BRWAIT: HALT
WLEN: HALT
RDYCHK: HALT
TKS: 177560
TKB: 177562
TPS: 177564
TPB: 177566
FNCCNT: HALT
INBUF1: HALT
SUSWR: MOV @#6,-(SP) ;SAVE VECTORS
MOV @#4,-(SP)
MOV #64,@#4 ;SET UP FOR TIMEOUT
CMP #-1,@SR ;REFERENCE HARDWARE SWITCH REGISTER
BEQ 65$
BR 66$

```

```

546 001122 022626
547 001124 012767 000176 177660
548 001132 012637 000004
549 001136 012637 000006
550 001142 022767 000176 177642
551 001150 001002
552 001152 004767 010646
553 001156 012777 000340 177630
554 001164 012767 001156 010542

```

```

645:  CMP      (SP)+,(SP)+      ;ADJUST STACK
655:  MOV      #SWREG,SR          ;POINT TO SOFTWARE SWITCH REG
665:  MOVL     (SE)+,R4             ;RESTORE VECTORS
      MOV      (SP)+,R6
      CMP      #SWREG,SR          ;IS S. REG USED
      BNE     BEGIN
      JSR     PC,ENTLU           ;ALLOW SWREG TO BE LOADED
BEGIN: MOV      #40,PSW          ;PROC. A LEVEL #7
      MOV      #BEGIN,RETURN

```

```

;*****
; TEST 0 CAN ALL DR11-B REG BE ADDRESSED WITHOUT ERROR?
;*****

```

```

555 001172 104400
556 001174 012767 001234 176602
557 001202 010700
558 001204 005277 177606
559 001210 010700
560 001212 005277 177602
561 001216 010700
562 001220 005277 177576
563 001224 010700
564 001226 005277 177572
565 001232 000401
566 001234 104000
567 001236 012767 000006 176540
568 001244 104400

```

```

SCOPE
MOV      #ERRA,BUSEPR          ;BUS ERROR VECTOR TO ERRA
MOV      %7,%0                ;PC TO R0
INC      @DRWC                 ;ADDRESS DRWC
MOV      %7,%0                ;PC TO R0
INC      @DRBA                 ;ADDRESS DRBA
MOV      %7,%0                ;PC TO R0
CLP      @DRST                 ;ADDRESS DRST
MOV      %7,%0                ;PC TO R0
INC      @DRDB                 ;ADDRESS DRDB
BR       .+4                   ;MADE IT - BRANCH OVER HALT
ERRA:  HLT
MOV      #6,BUSEPR            ;BUS ERROR, R0 HAS PC OF ERROR
SCOPE

```

```

;*****
; TEST 1 DOES RESET CLEAR DRWC?
;*****

```

```

569 001246 012767 000010 010454
570 001254 012777 177777 177534
571 001262 004767 010464
572 001266 000005
573 001270 005777 177522
574 001274 001401
575 001276 104000
576 001300 104400

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```

MOV      #10,ICOUNT
MOV      #-1,@DRWC            ;ALL ONES J DRWC
JSR      %7,CKSWR
RESET
TST      @DRWC                ;INIT
BEQ      .+4                   ;LOOKING FOR Z-BIT TO SET
HLT
SCOPE

```

```

;*****
; TEST2 DOES RESET CLEAR DRBA?
;*****

```

```

577 001302 104400
578 001304 012777 177777 177506
579 001312 004767 010434

```

```

SCOPE
MOV      #-1,@DRBA           ;ALL ONES TO DRBA
JSR      %7,CKSWR

```


MO1

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DZDRB.P11

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602 001316 000005 RESET ;INIT
603 001320 005777 177474 TST 3DRBA ;LOOKING FOR Z-BIT TO SET
604 001324 001401 BEQ .+4 ;DID DRBA GET CLEARED?
605 001326 104000 HLT ;DRBA NOT CLEAR

*****
; TEST3 CAN ALL DRWC BITS BE SET?
*****

613 001330 104400 SCOPE
614 001332 012767 004000 01C370 MOV #4000,ICOUNT
615 001340 012777 177777 177450 MOV #-1,3DRWC ;SET ALL BITS IN DRWC
616 001345 022777 177777 177442 CMP #-1,3DRWC ;LOOKING FOR Z-BIT TO SET
617 001354 001401 BEQ .+4 ;SEE IF ALL BITS GOT SET
618 001356 104000 HLT ;ALL BITS AREN'T SET

*****
; TEST4 CAN BITS 15-01 IN DRBA BE SET?
*****

625 001360 104400 SCOPE
626 001362 012777 177776 177430 MOV #-2,3DRBA ;SET BITS 15-01 IN DRBA
627 001370 022777 177776 177422 CMP #-2,3DRBA ;LOOKING FOR Z-BIT TO SET
628 001376 001401 BEQ .+4 ;SEE IF BITS 15-01 GOT SET
629 001400 104000 HLT ;BITS 15-01 AREN'T SET

*****
; TEST6 TEST THAT FNCT1 CAN BE SET AND CLEARED
*****

638 001402 104400 SCOPE
639 001404 052777 000002 177410 BIS #BIT1,3DRST ;SET FNCT1
640 001412 032777 000002 177402 BIT #BIT1,3DRST ;TEST FNCT1
641 001420 001001 BNE .+4 ;IS IT SET?
642 001422 104000 HLT ;FNCT1 IS CLEAR
643 001424 042777 000002 177370 BIC #BIT1,3DRST ;CLEAR FNCT1
644 001432 032777 000002 177362 BIT #BIT1,3DRST ;TEST FNCT1
645 001440 001401 BEQ .+4 ;WAS IT CLEAR
646 001442 104000 HLT ;FNCT1 WAS SET

*****
; TEST7 TEST THAT FNCT2 CAN BE SET AND CLEARED
*****

655 001444 104400 SCOPE
656 001446 052777 000004 177346 BIS #BIT2,3DRST ;SET FNCT2
657 001454 032777 000004 177340 BIT #BIT2,3DRST ;TEST FNCT2

```

```

001464 001001
001464 104000
001464 042777 000004 177326
001464 032777 000004 177320
001464 001401
001464 104000

```

```

BNE .+4 ;IS IT SET?
HLT ;FNCT2 IS CLEAR
BIC #BIT2,DRST ;CLEAR FNCT2
BIT #BIT2,DRST ;TEST FNCT2
BEQ .+4 ;WAS IT CLEAR?
HLT ;FNCT2 WAS SET

```

```

*****
TEST10 TEST THAT FNCT3 CAN BE SET AND CLEARED
*****

```

```

001464 000010 177204
001464 000010 177276
001464 000010 177254
001464 000010 177256

```

```

SCOPE
BIS #BIT3,DRST ;SET FNCT3
BIT #BIT3,DRST ;TEST FNCT3
BNE .+4 ;IS IT SET?
HLT ;FNCT3 IS CLEAR
BIC #BIT3,DRST ;CLEAR FNCT3
BIT #BIT3,DRST ;TEST FNCT3
BEQ .+4 ;WAS IT CLEAR?
HLT ;FNCT3 WAS SET

```

```

*****
TEST11 TEST THAT XBA16 CAN BE SET AND CLEARED
*****

```

```

001464 000020 177242
001464 000020 177234
001464 000020 177222
001464 000020 177214

```

```

SCOPE
BIS #BIT4,DRST ;SET XBA16
BIT #BIT4,DRST ;TEST XBA16
BNE .+4 ;IS IT SET?
HLT ;XBA16 IS CLEAR
BIC #BIT4,DRST ;CLEAR XBA16
BIT #BIT4,DRST ;TEST XBA16
BEQ .+4 ;IS IT CLEAR?
HLT ;XBA16 WAS SET

```

```

*****
TEST12 TEST THAT XBA17 CAN BE SET AND CLEARED
*****

```

```

001464 000040 177200
001464 000040 177172
001464 000020 177150
001464 000020 177152

```

```

SCOPE
BIS #BIT5,DRST ;SET XBA17
BIT #BIT5,DRST ;TEST XBA17
BNE .+4 ;IS IT SET?
HLT ;XBA17 IS CLEAR
BIC #BIT4,DRST ;CLEAR XBA17
BIT #BIT4,DRST ;TEST XBA17
BEQ .+4 ;IS IT CLEAR?
HLT ;XBA17 WAS SET

```

```

*****
TEST13 TEST THAT IE CAN BE SET AND CLEARED
*****

```

```

001464 000000 177136
001464 000000 177130

```

```

SCOPE
BIS #BIT6,DRST ;SET IE
BIT #BIT6,DRST ;TEST IE

```


00000000 104400
00000000 012777
00000000 032777
00000000 001010
00000000 004767
00000000 000005
00000000 032777
00000000 001001
00000000 104000
00000000 012777
00000000 032777
00000000 000240
00000000 042777
00000000 000401
00000000 104000

004000 007140
000340 176216
000200 176216
007140
000200 176200
002654 176176
000100 176160
000100 176150
000100 176150

SCOPE
MOV #4000,ICOUNT
MOV #340,IPSW :STATUS AT LEVEL 7
BIT #BIT7,DRST :CHECK READY BIT
BNE P6INV :IS IT SET
JSR %7,CKSWR
RESET :INIT TO SET READY
BIT #BIT7,DRST :SEE IF READY IS SET NOW
BNE .+4 :IS READY SET?
HLT :READY CAN'T BE SET BY INIT
P7INV: MOV #P7ERR,DRINV :SET UP INT VECTOR
BIS #BIT6,DRST :SET IE
NOP
BIC #BIT6,DRST ;DR11-B DIDN'T INTERRUPT - CLEAR IE
BR .+4
P7ERR: HLT ;DR11-B INTERRUPTED, BUT IT SHOULDN'T HAVE

TEST26 TEST THAT DR11-B DOES NOT INTERRUPT WITH PROC AT LEVEL 6

00000000 104400
00000000 012777
00000000 032777
00000000 001010
00000000 004767
00000000 000005
00000000 032777
00000000 001001
00000000 104000
00000000 012777
00000000 032744
000100 176070
000100 176060
000100 176060
000401
104000

000300 176126
000200 176126
007050
000200 176110
002744 176106
000100 176070
000100 176060
000100 176060

SCOPE
MOV #300,IPSW :STATUS AT LEVEL 6
BIT #BIT7,DRST :CHECK READY BIT
BNE P6INV :IS IT SET?
JSR %7,CKSWR
RESET :INIT TO SET READY
BIT #BIT7,DRST :SEE IF READY IS SET NOW
BNE .+4 :IS READY SET?
HLT :READY CAN'T BE SET BY INIT
P6INV: MOV #P6ERR,DRINV :SET UP INT VECTOR
BIS #BIT6,DRST :SET IE
NOP
BIC #BIT6,DRST ;DR11-B DIDN'T INTERRUPT - CLEAR IE
BR .+4
P6ERR: HLT ;DR11-B INTERRUPTED, BUT IT SHOULDN'T HAVE

TEST27 TEST THAT DR11-B DOES NOT INTERRUPT WITH PROC AT LEVEL 5

00000000 104400
00000000 012777
00000000 032777
00000000 001010
00000000 004767
00000000 000005
00000000 032777
00000000 001001
00000000 104000
00000000 012777
00000000 032777
00000000 000240
00000000 042777
00000000 000401
00000000 104000

000240 176036
000200 176036
006760
000200 176020
003034 176016
000100 176000
000100 175770
000100 175770

SCOPE
MOV #240,IPSW :STATUS AT LEVEL 5
BIT #BIT7,DRST :CHECK READY BIT
BNE P5INV :IS IT SET?
JSR %7,CKSWR
RESET :INIT TO SET READY
BIT #BIT7,DRST :SEE IF READY IS SET NOW
BNE .+4 :IS IT SET?
HLT :RDY CAN'T BE SET BY INIT
P5INV: MOV #P5ERR,DRINV :SET UP INT VECTOR
BIS #BIT6,DRST :SET IE
NOP
BIC #BIT6,DRST ;DR11-B DIDN'T INTERRUPT - CLEAR IE
BR .+4
P5ERR: HLT ;DR11-B INTERRUPTED, BUT IT SHOULDN'T HAVE


```

003304 104400
003306 005777 175510
003312 100027
003314 032777 020000 175500
003322 001401
003324 104000
003326 032777 040000 175466
003334 001410
003336 042777 040000 175456
003344 032777 040000 175450
003352 001401
003354 104000
003356 005077 175436
003362 005777 175434
003366 001401
003370 104000
003372 012777 177777 175416
003400 012777 001034 175412
003406 005077 175412
003412 012767 052525 175414
003420 012777 003464 175404
003426 012777 000005 175372
003434 005077 175354
003440 012777 000101 175354
003446 005067 000002
003452 005227 000001
003456 001375
003460 104000
003462 000424
003464 004767 003312
003470 005777 175322
003474 001401
003476 104000
003500 022777 001036 175312
003506 001401
003510 104000
003512 022777 052525 175304
003520 001401
003522 104000
003524 004767 003162
003530 022626
003532 000403
003534 005077 175262
003540 000662

SCOPE
TNPRI: TST @DRST ;CHECK ERROR BIT
      BFL NPRDY ;IS IT CLEAR?
      BIT @BIT13,@DRST ;CHECK ATTN
      BEQ .+4 ;IS ATTN CLEAR
      HLT ;ATTN IS SET
      SIT @BIT14,@DRST ;CHECK NEX
      BEQ N1413 ;IS NEX CLEAR?
      BIC @BIT14,@DRST ;TRY TO CLEAR NEX
      BIT @BIT14,@DRST ;CHECK AGAIN
      BEQ .+4 ;NEX STILL SET
      HLT ;NEX CAN'T BE CLEARED BY MOVING A 0 TO IT
N1413: CLR @DRBA ;TRY TO CLEAR BACF
      TST @DRST ;CHECK ERROR BIT AGAIN
      BEQ .+4 ;IS IT CLEAR
      HLT ;ERROR CAUSED BY SOMETHING OTHER THAN NEX,ATTN, OR BACF
NPRDY: MOV #-1,@DRWC ;SET UP FOR 1 TRANSFER
      MOV @NPR1,@DRBA ;TRANSFER FROM BUS ADDRESS IN NPR1
      CLR @DRDB ;GET READY TO RECEIVE DATA
      MOV @52525,NPR1 ;SET UP TRANSFER DATA
      MOV @INTB,@DRINV ;INTERRUPT VECTOR TO INTB
      MOV @5,@DRVS ;INTERRUPT PRIORITY TO LEVEL 5
      CLR @PSW ;LET THE DR11-B INTERRUPT
      MOV @101,@DRST ;IE AND DO TO DRST
      CLR @5+2 ;WAIT FOR NPR AND INTERRUPT
      INC @1
      BNE @3
      HLT ;NO DR11-B INTERRUPT
INTB: BR T33CLR ;CLEAR IE
      JSR %7,ERRCHK ;TEST DRWC
      TST @DRWC ;IS DRWC EQUAL TO ZERO?
      BEQ .+4 ;DRWC NOT EQUAL TO ZERO
      HLT ;COMPARE CORRECT DRBA WITH DRBA
      CMP @NPR1+2,@DRBA ;IS THE DRBA CORRECT?
      BEQ .+4 ;DRBA IS WRONG
      HLT ;CHECK FOR CORRECT DATA
      CMP @52525,@DRDB ;DATA GET TRANSFERRED?
      BEQ .+4 ;BAD DATA IN DRDB
      HLT
      JSR %7,NORMAL ;RESTORE STACK
      CMP (%6)+,(%6)+ ;GO TO NEXT TEST (NPR OUT)
      BR TNPRC ;CLEAR IE
T33CLR: CLR @DRST ;TRY TEST AGAIN
      BR TNPRI

:*****
: TEST 34 TEST FOR 1 DATO NPR TRANSFER (WITH 1968 IN USER SLOTS)
:*****
TNPRO: SCOPE
      MOV #-1,@DRWC ;SET UP FOR 1 TRANSFER
      MOV @NPR1,@DRBA ;TRANSFER TO BUS ADDRESS IN NPR1
      CLR NPR1 ;GET READY TO RECEIVE DATA
      MOV @52525,@DRDB ;SET UP TO TRANSFER DATA
      MOV @INTC,@DRINV ;INTERRUPT VECTOR TO INTC
      MOV @DRINL,@DRVS ;INTERRUPT STATUS TO LEVEL DRINL
      CLR @PSW ;PRCC STATUS TO ZERO
      MOV @103,@DRST ;IE, FNCT1(C1 CONTROL), AND DO TO DRST

```



```

1050 003620 005067 000002          CLR      15+2          ;WAIT FOR NPR AND INTER
1051 003624 005227 000001          IS:      INC          #1
1052 003630 001375          BNE      15
1053 003632 104000          HLT
1054 003634 000424          BR       T34CLR      ;NO DR11-B INTERRUPT
1055 003636 004767 003140          INTC:   JSR      .7,ERRCHK ;CLEAR IE
1056 003642 005777 175150          TST     @DRWC
1057 003646 001401          BEQ     .+4          ;TEST DRWC
1058 003650 104000          HLT          ;IS DRWC EQUAL TO ZERO?
1059 003652 022777 001036 175140        CMP     #NPR1+2,@DRBA ;DRWC EQUAL TO ZERO
1060 003660 001401          BEQ     .+4          ;COMPARE CORRECT DRBA WITH DRBA
1061 003662 104000          HLT          ;IS THE DRBA CORRECT?
1062 003664 026727 175144 052525        CMP     NPR1,#52525  ;DRBA IS WRONG
1063 003670 001401          BEQ     .+4          ;CHECK FOR CORRECT DATA
1064 003672 104000          HLT          ;CORRECT DATA TRANSFERPED?
1065 003674 104000          HLT          ;BAD DATA
1066 003676 004767 003010          JSR     .7,NORMAL
1067 003702 022626          CMP     (%6)+,(%6)+ ;RESTORE STACK
1068 003704 000403          BR
1069 003706 025077 175110        T34CLR: CLR     @DRST  ;GO TO NEXT TEST
1070 003712 000713          BR      TNPRO       ;CLEAR IE
1071
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1073
1074
1075 003714 104400          ;*****
1076 003716 012767 000020 175120        : TEST 35 STRING OF 10 DATI'S (WITH M968 IN USER SLOTS)
1077 003724 004767 002524          ;*****
1078 003730 006267 175110          T35:  SCOPE
1079 003734 016767 175104 175110        MOV     #20,BUFLEN  ;LENGTH OF BUFFER=20
1080 003742 005467 175104          JSR     %7,LODBUF   ;LOAD THE BUFFER WITH INCREMENTING PATTERN
1081 003746 015777 175100 175042        ASR     BUFLN       ;BUFLN=10
1082 003754 016777 175060 175036        MOV     BUFLN,WLEN  ;PREPARE NUMBER FOR DRWC
1083 003762 012777 177777 175034        NEG     WLEN        ;2'S COMPLEMENT OF BUFLN
1084 003770 012777 006556 175034        MOV     WLEN,@DRWC ;SET UP DRWC
1085 003776 015777 175026 175022        MOV     INBUF,@DRBA ;SET UP DRBA
1086 004004 005077 175004          MOV     #-1,@DRDB  ;MAINT AIDE
1087 004010 012777 000101 175004        MOV     #INTA,@DRINV ;INT VECTOR TO INTA
1088 004016 000777          CLR     @PSW       ;INT VECTOR TO PRIORITY DRINL
1089 004020 022777 000007 174776        MOV     #101,@CRST ;LET THE DR11-B INTERRUPT
1090 004026 001401          BR      .          ;IE AND DO TO DRST
1091 004030 104000          CMP     #7,@DRDB   ;WAIT FOR INTERRUPT
1092
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1096 004032 104400          ;*****
1097 004034 012767 000020 175002        : TEST 35 STRING OF 10 DATO'S (WITH M968 IN USER SLOTS)
1098 004042 004767 002406          ;*****
1099 004046 006267 174772          SCOPE
1100 004052 016767 174766 174772        MOV     #20,BUFLEN  ;LENGTH OF BUFFER=20
1101 004060 005467 174766          JSR     %7,LODBUF   ;LOAD THE BUFFER WITH INCREMENTING PATTERN
1102 004064 016777 174762 174724        ASR     BUFLN       ;BUFLN=10
1103 004072 016777 174742 174720        MOV     BUFLN,WLEN  ;PREPARE NUMBER FOR DRWC
1104 004100 012777 052525 174716        NEG     WLEN        ;2'S COMPLEMENT OF BUFLN
1105 004106 012777 006556 174716        MOV     WLEN,@DRWC ;SET UP DRWC
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1106 004114 016777 174710 174704
1107 004112 005077 174666
1108 004126 012777 000103 174666
1109 004134 000777
1110 004136 004767 002572
1111
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1115 004142 104400
1116 004144 012767 000200 174672
1117 004152 004767 002276
1118 004156 016767 174562 174666
1119 004164 005467 174662
1120 004170 016777 174656 174620
1121 004176 016777 174636 174614
1122 004207 012777 177777 174512
1123 004212 012777 006556 174612
1124 004220 016777 174604 174600
1125 004226 005077 174562
1126 004232 012777 000101 174562
1127 004240 000777
1128 004242 022777 000177 174554
1129 004250 001401
1130 004252 104000
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1134 004254 104400
1135 004256 012767 000201 174560
1136 004264 004767 002164
1137 004270 005367 174550
1138 004274 016767 174544 174550
1139 004302 005467 174544
1140 004306 016777 174540 174502
1141 004314 016777 174520 174476
1142 004322 012777 052525 174474
1143 004330 012777 006556 174474
1144 004336 016777 174466 174462
1145 004344 005077 174444
1146 004350 012777 000103 174444
1147 004356 000777
1148 004360 004767 002350
1149
1150
1151
1152
1153 004364 104400
1154 004366 012777 177776 174422
1155 004374 016777 174436 174416
1156 004402 012777 004436 174422
1157 004410 016777 174414 174410
1158 004416 005077 174372
1159 004422 012777 000163 174372
1160 004430 005237 177560
1161 004434 104000

```

```

MOV DRINL,DRVS ;INTERRUPT VECTOR TO PRIORITY DRINL
CLR DRPSW ;LET THE DR11-B INTERRUPT
MOV #103,DRST ;IE, FNCT1(C1 CONTROL), AND GO TO DRST
BR ;WAIT FOR INTERRUPT
JSR %7.DATOCK ;CHECK INBUF

;*****
; TEST 37 STRING OF 200 DATI'S
;*****
SCOPE
MOV #200,BUFLEN ;LENGTH OF BUFFER=200
JSR %7.LODBUF ;LOAD THE BUFFER WITH INCREMENTING PATTERN
MOV BUFLEN,WLEN ;PREPARE NUMBER FOR DRWC
NEG WLEN ;2'S COMPLEMENT OF BUFLEN
MOV WLEN,DRWC ;SET UP DRWC
MOV INBUF,DRBA ;SET UP DRBA
MOV #-1,DRDB ;MAINT AIDE
MOV #INTA,DRINV ;INT VECTOR TO INTA
MOV DRINL,DRVS ;INT VECTOR TO PRIORITY DRINL
CLR DRPSW ;LET THE DR11-B INTERRUPT
MOV #101,DRST ;IE AND GO TO DRST
BR ;WAIT FOR INTERRUPT
CMP #177,DRDB ;CHECK THAT WORD #200 OF INBUF IS IN DRBA
BEQ .+4 ;IS IT?
HLT ;BAD DATA IN DRDB

;*****
; TEST 40 STRING OR 200 DATO'S
;*****
SCOPE
MOV #201,BUFLEN ;LENGTH OF BUFFER=201
JSR %7.LODBUF ;LOAD THE BUFFER WITH INCREMENTING PATTERN
DEC BUFLEN ;BUFLEN=200
MOV BUFLEN,WLEN ;PREPARE NUMBER FOR DRWC
NEG WLEN ;2'S COMPLEMENT OF BUFLEN
MOV WLEN,DRWC ;SET UP DRWC
MOV INBUF,DRBA ;SET UP DRBA
MOV #52525,DRDB ;SET UP DRDB
MOV #INTA,DRINV ;INTERRUPT VECTOR TO INTA
MOV DRINL,DRVS ;INTERRUPT VECTOR TO PRIORITY DRINL
CLR DRPSW ;LET THE DR11-B INTERRUPT
MOV #103,DRST ;IE, FNCT1, AND GO TO DRST
BR ;WAIT FOR INTERRUPT
JSR %7.DATOCK ;CHECK INBUF

;*****
; TEST 42 TEST THAT DOING A DATO TO THE DIODE MEMORY CAUSES NEX
;*****
SCOPE
MOV #-2,DRWC ;SET UP DRWC
MOV DIOMEM,DRBA ;SET UP DRBA
MOV #NEXCHK,DRINV ;INTERRUPT VECTOR TO NEXCHK
MOV DRINL,DRVS ;INTERRUPT STATUS TO LEVEL DRINL
CLR DRPSW ;LET THE DR11-B INTERRUPT
MOV #163,DRST ;IE, FNCT1, XBA17, XBA16, AND GO TO DRST
INC #177560 ;WAIT FOR INTERRUPT
HLT ;NO DR11-B INTERRUPT

```

```

1162 004436 005777 17436J NEXCHK: TST @DRST ;TEST DRST
1163 004442 001001 BNE .+4 ;ERROR SET?
1164 004444 104000 HLT ;ERROR NOT SET
1165 004446 105777 174350 TSTB @DRST ;TEST FOR READY
1166 004452 001001 BNE .+4 ;READY SET?
1167 004454 104000 HLT ;READY ISN'T SET
1168 004456 032777 040000 174336 BIT @BIT14,@DRST ;CHECK NEX
1169 004464 001001 BNE .+4 ;NEX SET?
1170 004466 104000 HLT ;NEX IS CLEAR
1171 004470 022626 CMP (%)+,(%)+ ;RESTORE THE STACK
1172 004472 004767 002214 JSR @7,NORMAL

:*****
: TEST 43 TEST THAT BAOF FORCES ERROR AND READY AND THAT BAOF IS
: CLEARED BY CLEARING THE DRBA OR A RESET
:*****
1178 004476 104400 SCOPE
1179 004500 012767 000010 005222 MOV @10,ICOUNT
1180 004506 012777 177760 174302 MOV @-20,@DRWC ;SET UP DRWC
1181 004514 012777 177776 174276 MOV @-2,@DRBA ;SET UP DRBA FOR PROC STATUS ADDRESS
1182 004522 012777 004556 174302 MOV @BAOFCK,@DRINV ;INTERRUPT VECTOR TO BAOFCK
1183 004530 016777 174274 :74270 MOV DRINL,@DRVS ;INTERRUPT STATUS TO LEVEL DRINL
1184 004536 005077 174252 CLR @PSW ;LET THE DR11-B INTERRUPT
1185 004542 012777 000163 174252 MOV @163,@DRST ;I.E. FNCT1, XBA17, XBA16, AND GO TO DRST
1186 004550 005237 177560 INC @177560 ;WAIT FOR INTERRUPT
1187 004554 104000 HLT ;NO DR11-B INTERRUPT
1188 004556 022626 174236 BAOFCK: CMP (%)+,(%)+ ;RESTORE THE STACK
1189 004560 005777 TST @DRST ;TEST DRST
1190 004564 100401 BMI .+4 ;ERROR SET?
1191 004566 104000 HLT ;ERROR NOT SET
1192 004570 105777 174226 TSTB @DRST ;TEST FOR READY
1193 004574 100401 BMI .+4 ;READY SET?
1194 004576 104000 HLT ;READY ISN'T SET
1195 004600 042777 040000 174214 BIT @BIT14,@DRST ;CLEAR NEX
1196 004606 032777 060000 174206 BIT @60000,@DRST ;CHECK NEX AND ATTN
1197 004614 001401 BEQ .+4 ;ARE THEY CLEAR?
1198 004616 104000 HLT ;NEX AND/OR ATTN IS SET
1199 004620 005777 174176 TST @DRST ;TEST FOR ERROR
1200 004624 100401 BMI .+4 ;IS ERROR SET?
1201 004626 104000 HLT ;ERROR IS CLEAR
1202 004630 005077 174164 CLR @DRBA ;CLEAR BAOF
1203 004634 005777 174162 TST @DRST ;CHECK ERROR
1204 004640 100001 BPL .+4 ;SHOULD BE CLEAR
1205 004642 104000 HLT ;CLEARING DRBA DIDN'T CLEAR BAOF
1206
1207 004644 012777 177776 174146 MOV @-2,@DRBA ;SET UP DRBA FOR PROC STATUS ADDRESS
1208 004652 012777 004706 174152 MOV @BAOFCK1,@DRINV ;INTERRUPT VECTOR TO BAOFCK1
1209 004660 016777 174144 174140 MOV DRINL,@DRVS ;INTERRUPT STATUS TO LEVEL DRINL
1210 004666 005077 174122 CLR @PSW ;LET THE DR11-B INTERRUPT
1211 004672 012777 000163 174122 MOV @163,@DRST ;I.E., XBA17, XBA16, FNCT1, AND GO TO DRST
1212 004700 005237 177560 INC @177560 ;WAIT FOR INTERRUPT
1213 004704 104000 HLT ;NO DR11-B INTERRUPT
1214 004706 022626 174106 BAOFCK1: CMP (%)+,(%)+ ;RESTORE THE STACK
1215 004710 005777 TST @DRST ;TEST DRST
1216 004714 100401 BMI .+4 ;ERROR SET?
1217 004716 104000 HLT ;ERROR NOT SET

```

```

1218 004720 105777 174076
1219 004724 100401
1220 004726 104000
1221 004730 042777 040000 174064
1222 004736 032777 060000 174056
1223 004744 001401
1224 004746 104000
1225 004750 005777 174046
1226 004754 100401
1227 004756 104000
1228 004760 004767 004766
1229 004764 000005
1230 004766 005777 174030
1231 004772 000001
1232 004774 104000
1233 004776 004767 001710
1234
1235
1236
1237
1238 005002 104400
1239 005004 012767 000010 004716
1240 005012 012777 177777 174004
1241 005020 004767 004726
1242 005024 000005
1243 005026 005777 173772
1244 005032 001401
1245 005034 104000
1246
1247
1248
1249
1250 005036 104400
1251 005040 012767 004000 004662
1252 005046 012777 177777 173750
1253 005054 022777 177777 173742
1254 005062 001401
1255 005064 104000
1256
1257
1258
1259
1260 005066 104400
1261 005070 012777 052525 173726
1262 005076 022777 052525 173720
1263 005104 001401
1264 005106 104000
1265 005110 012777 125252 173706
1266 005116 022777 125252 173700
1267 005124 001401
1268 005126 104000
1269
1270
1271
1272
1273 005130 104400

```

```

TSTB 2DRST ;TEST FOR READY
BMT .+4 ;READY SET?
HLT ;READY ISN'T SET
BIC #BIT14,2DRST ;CLEAR NEX
BIT #60000,2DRST ;CHECK NEX AND ATTN
BEQ .+4 ;ARE THEY CLEAR?
4 ;NEX AND/OR ATTN IS SET
TST 2DRST ;TEST FOR ERROR
BMT .+4 ;IS ERROR SET?
HLT ;ERROR IS CLEAR
JSR %7,CKSWR
RESET ;INIT
TST 2DRST ;CHECK ERROR
BPL .+4 ;SHOULD BE CLEAR
HLT ;RESET DIDN'T CLEAR BAOF
JSR %7,NORMAL

:*****
: TEST 44 TEST THAT RESET CLEARS DRDB
:*****
SCOPE
OV #10,ICOUNT
MOV #-1,2DRDB ;ALL ONES TO DRDB
JSR %7,CKSWR
RESET ;INIT
TST 2DRDB ;LOOKING FOR Z-BIT TO SET
BEQ .+4 ;DID DRDB GET CLEARED?
HLT ;DRDB NOT CLEAR

:*****
: TEST 45 TEST THAT ALL DRDB BITS CAN BE SET
:*****
SCOPE
MOV #4000,ICOUNT
MOV #-1,2DRDB ;SET ALL BITS IN DRDB
CMP #-1,2DRDB ;LOOKING FOR Z-BIT TO SET
BEQ .+4 ;SEE IF ALL BITS GOT SET
HLT ;ALL DRDB BITS AREN'T SET

:*****
: TEST 46 TEST THAT DRDB CAN HOLD ALTERNATE ONE'S AND ZERO'S
:*****
SCOPE
MOV #052525,2DRDB ;ALT 0'S AND 1'S TO DRDB
CMP #052525,2DRDB ;LOOKING FOR Z-BIT TO SET
BEQ .+4 ;DOES DRDB HAVE THE CORRECT PATTERN?
HLT ;DRDB IS WRONG
MOV #125252,2DRDB ;ALT 1'S AND 0'S TO DRDB
CMP #125252,2DRDB ;LOOKING FOR Z-BIT TO SET
BEQ .+4 ;DOES DRDB HAVE THE CORRECT PATTERN
HLT ;DRDB IS WRONG

:*****
: TEST 47 INCREMENTING PATTERN TO WRAP-AROUND IN DRDB
:*****
SCOPE

```



```

1274 005132 005067 004572          CLR      ICOUNT
1275 005133 005001          CLR      %1          ;SET-UP
1276 005134 005077 173660      CLR      @DRDB      ;SET-UP
1277 005140 005077 173654      INCDB:  CMP      %1,@DRDB ;SEE IF THEY ARE EQUAL
1278 005144 020177 173654          BEQ      .+4          ;ARE THEY EQUAL?
1279 005150 001401          HLT      ;THEY'RE NOT EQUAL
1280 005152 104000          HLT      ;THEY'RE NOT EQUAL
1281 005154 005277 173644      INC      @DRDB      ;GET NEXT NUMBER
1282 005160 005201          INC      %1          ;GET NEXT NUMBER
1283 005162 001370          BNE      INCDB      ;DONE WITH TEST? IF NOT CONTINUE
1284
1285 ;*****
1286 ;TEST 50 TEST THAT RESET SETS READY AND CLEARS ALL OTHER
1287 ;DRST BITS (WITH M968 INSERTED)
1288 ;*****
1289 005164 104400          SCOPE
1290 005166 004767 004560      JSR      %7,CKSWR
1291 005172 000005          RESET
1292 005174 032777 000200 173620  BIT      #BIT7,@DRST ;INIT
1293 005202 001001          BNE      .+4          ;CHECK DRST
1294 005204 104000          HLT      ;IS READY SET?
1295 005206 032777 177577 173606  BIT      #177577,@DRST ;READY IS CLEAR
1296 005214 001401          BEQ      .+4          ;CHECK DRST
1297 005216 104000          HLT      ;ARE THEY ALL CLEAR?
1298 ;*****
1299 ;TEST 51 TEST THAT BA00 READS AS A ZERO WITH MAINT BOARD INSERTED
1300 ;*****
1301 005220 104400          SCOPE
1302 005222 012767 004000 004500  MOV      #4000,ICOUNT
1303 005230 032777 000001 173562  BIT      #BIT0,@DRBA ;TEST BIT 0 OF DRBA
1304 005236 001401          BEQ      .+4          ;IS IT CLEAR?
1305 005240 104000          HLT      ;BA00 IS SET
1306
1307
1308
1309 ;*****
1310 ;TEST 52 TEST THAT GO CLEARS READY
1311 ;*****
1312 005242 104400          SCOPE
1313 005244 012767 004000 004456  MOV      #4000,ICOUNT
1314 005252 012777 177600 173536  MOV      #-200,@DRWC ;SET-UP DRWC
1315 005260 016777 173554 173532  MOV      INBUF,@DRPA ;SET-UP DRPA
1316 005266 105777 173530          TSTB    @DRST      ;CHECK READY
1317 005272 100401          BMI     .+4          ;IS READY SET?
1318 005274 104000          HLT      ;READY IS CLEAR
1319 005276 012777 000011 173516  MOV      #11,@DRST ;FNCT3 (NON-BURST) AND GO TO DRST
1320 005304 105777 173512          TSTB    @DRST      ;CHECK READY
1321 005310 100001          BPL     .+4          ;IS READY CLEAR?
1322 005312 104000          HLT      ;READY IS STILL SET
1323 005314 005067 173534          CLR     RDYCHK      ;CLEAR READY CHECK
1324 005320 105777 173476      TSTRDY: TSTB    @DRST ;CHECK READY
1325 005324 100406          BMI     DONE        ;CHECKING TIME FOR READY TO BE SET
1326 005326 062767 000004 173520  ADD     #4,RDYCHK    ;IF SET GO TO DONE
1327 005334 100401          BMI     .+4          ;CHECKING TIME FOR READY TO BE SET
1328 005336 000770          BR     TSTRDY       ;IF RDYCHK GETS NEGATIVE IT TOOK TOO LONG
1329 005340 104000          HLT      ;CHECK AGAIN
;READY GOT CLEARED BUT NEVER SET AGAIN

```

```

1330 005342 000240
1331
1332
1333
1334
1335 005344 104400
1336 005346 012777 177760 173442
1337 005354 016777 173456 173436
1338 005362 012777 005416 173442
1339 005370 012777 000200 173430
1340 005376 005077 173412
1341 005402 012777 000163 173412
1342 005410 005277 173442
1343 005414 104000
1344 005416 005777 173400
1345 005422 100401
1346 005424 104000
1347 005426 012777 005474 173376
1348 005434 005077 173360
1349 005440 042777 000062 173354
1350 005446 012777 177777 173342
1351 005454 005277 173342
1352 005460 005067 000002
1353 005464 005227 000001
1354 005470 001375
1355 005472 104000
1356 005474 005777 173322
1357 005500 100401
1358 005502 104000
1359
1360 005504 062706 000010
1361 005510 004767 001176
1362
1363
1364
1365
1366 005514 104400
1367 005516 012767 000200 173320
1368 005524 004767 000724
1369 005530 016767 173310 173314
1370 005536 005467 173310
1371 005542 016777 173304 173246
1372 005550 016777 173264 173242
1373 005556 012777 177777 173240
1374 005564 012777 006556 173240
1375 005572 016777 173232 173226
1376 005600 005077 173210
1377 005604 012777 000111 173210
1378 005612 005267 173232
1379 005616 032767 000001 173224
1380 005624 001403
1381 005626 000001
1382 005630 000240
1383 005632 000401
1384 005634 000777
1385 005636 022777 000177 173160

```

```

DONE: MOP ;GO TO NEXT TEST
;*****
;TEST 55 TEST THAT GIVING A DO WITHOUT CLEARING A PREVIOUS ERROR
;CAUSES ANOTHER INTERRUPT
;*****
SCOPE
MOV #20,DRWC ;SET-UP DRWC
MOV DIOMEM,DRBA ;SET-UP DRBA
MOV #ERRD0,DRINV ;INTERRUPT VECTOR TO ERRD0
MOV #200,DRVS ;INTERRUPT STATUS TO LEVEL 4
CLR DRPSW ;LET THE DR11-B INTERRUPT
MOV #163,DRST ;IE, XBA17,XBA16, FNCT1 AND GO TO DRST
INC DRTKS ;WAIT FOR INTERRUPT
HLT ;NO DR11-B INTERRUPT
ERRD0: TST DRST ;TEST DRST
BMI .+4 ;ERROR SET?
HLT ;ERROR IS CLEAR - SHOULD HAVE NEX
MOV #ERRD01,DRINV ;INTERRUPT VECTOR TO ERRD01
CLR DRBA ;PREVENT CAUSING ANOTHER ERROR
BIC #62,DRST ;CLEAR XBA17, XBA16, AND FNCT1
MOV #-1,DRWC ;SET-UP DRWC
INC DRST ;DO TO DRST
CLR DRPSW
IS: INC IS+2
BNE IS
HLT ;NO DR11-B INTERRUPT
ERRD01: TST DRST ;CHECK ERROR
BMI .+4 ;ERROR SET?
HLT ;ERROR IS CLEAR - SHOULD BE SET BECAUSE
;PREVIOUS ERROR WAS NOT CLEARED
ADD #10,%6 ;REPOSITION THE STACK
JSR %7,NORMAL
;*****
;TEST 56 STRING OF 200 DATI'S NON-BURST MODE
;*****
SCOPE
MOV #200,BUFLEN ;LENGTH OF BUFFER=200
JSR %7,LODBUF ;LOAD THE BUFFER WITH INCREMENTING PATTERN
MOV BUFLN,WCLN ;PREPARE NUMBER FOR DRWC
NEG WCLN ;2'S COMPLEMENT OF BUFLN
MOV WCLN,DRWC ;SET-UP DRWC
MOV INBUF,DRBA ;SET-UP DRBA
MOV #-1,DRD0B ;MAINT AIDE
MOV #INTA,DRINV ;INT VECTOR TO INTA
MOV DRINL,DRVS ;INT VECTOR TO PRIORITY DRINL
CLR DRPSW ;LET THE DR11-B INTERRUPT
MOV #111,DRST ;IE, FNCT3, AND DO TO DRST
INC BRWAIT ;USE A WAIT OR BR. INSTRUCTION
BIT #BIT0,BRWAIT ;SEE WHICH ONE
BEQ DATINB ;BIT 0 CLEAR=BR.
WAIT ;WAIT FOR INTERRUPT
BR .+4
DATINB: BR
CMP #177,DRD0B ;CHECK THAT WORD #200 OF INBUF IS IN DR9A

```

```

005644 104401
005646 104000
005650 104400
005652 012767 000201 173164
005660 004767 000570
005664 005367 173154
005670 016767 173150 173154
005676 005467 173150
005702 016777 173144 173106
005710 016777 173124 173102
005716 012777 052525 173100
005724 012777 005556 173100
005732 016777 173072 173066
005740 005077 173050
005744 012777 000113 173050
005752 005267 173072
005756 032767 000001 173064
005764 001403
005766 000001
005770 000240
005772 000401
005774 000777
005776 004767 000732
006002 104400
006004 012767 000010 173032
006012 016777 173022 173000
006020 004767 000430
006024 004767 000462
006030 005077 172766
006034 012767 000001 173024
006042 012767 000001 172774
006050 016767 172764 173012
006056 012777 006556 172746
006064 016777 172740 172734
006072 005077 172716
006076 012777 177777 172712
006104 052777 010101 172710
006112 000001
006114 000240
006116 117701 172700
006122 042701 000600
006126 006201
006130 126701 172732
006134 001401
006136 104000
006140 005267 172722
006144 022767 000010 172714
006152 001404

```

```

      BEQ      .+4      ; IS IT?
      HLT
      ;BAD DATA IN DRDB

:*****
:      TEST 57 STRING OF 200 DATO'S NON-BURST MODE
:*****
      SCOPE
      MOV      #201, BUFLN      ; LENGTH OF BUFFER=201
      JSR      %7, LOOBUF      ; LOAD THE BUFFER WITH INCREMENTING PATTERN
      DEC      BUFLN           ; BUFLN=200
      MOV      BUFLN, WCLN     ; PREPARE NUMBER FOR DRWC
      NEG      WCLN           ; 2'S COMPLEMENT OF BUFLN
      MOV      WCLN, @DRWC     ; SET UP DRWC
      MOV      INBUF, @DRBA    ; SET UP DRBA
      MOV      #52525, @DRDB   ; SET UP DRDB
      MOV      #INTA, @DRINV   ; INTERRUPT VECTOR TO INTA
      MOV      DRINL, @DRVS    ; INTERRUPT VECTOR TO PRIORITY DRINL
      CLR      @PSW           ; LET THE DR11-B INTERRUPT
      MOV      #113, @DRST     ; IE, FNCT3, FNCT1, AND DO TO DRST
      INC      BRWAIT         ; USE A WAIT OR BR. INSTRUCTION
      BIT      #BIT0, BRWAIT   ; BIT 0 CLEAR=BR.
      BEQ      DATONB
      WAIT
      NOP
      BR      .+4
      DATONB: BR
      JSR      %7, DATOCK      ; CHECK INBUF

:*****
:      TEST 60 TEST THAT FUNCTION BITS INCREMENT WITH MAINT MODE TRANSFERS
:*****
      SCOPE
      MOV      #10, BUFLN     ; SET-UP BUFLN FOR LOOBUF AND CHKBUFF
      MOV      INBUF, @DRBA   ; SET-UP DR2A
      JSR      %7, LOOBUF     ; LOAD INBUF
      JSR      %7, CHKBFF    ; LOAD CHKBUFF
      CLR      @DRST         ; INIT FOR STARTING
      MOV      #1, FNCCNT     ; GET READY FOR CHECKING
      MOV      #1, BUFLN     ; CHANGE IS NECESSARY FOR INTA ROUTINE
      MOV      INBUF, INBUF1  ; SAVE INBUF
      MOV      #INTA, @DRINV  ; INTERRUPT VECTOR TO INTA
      MOV      DRINL, @DRVS  ; INTERRUPT VECTOR PRIORITY TO DRINL
      CLR      @PSW         ; LET THE DR11-B INTERRUPT
      MOV      #-1, @DRWC    ; SET-UP FOR I TRANSFER
      BIS      #10101, @DRST ; MAINT IE AND DC TO DRST
      WAIT
      NOP
      MOV      @DRST, %1     ; FAKE-OUT RETURN ADDRESS CHANGING
      BIC      #600, %1     ; LOWER BYTE OF DRST TO R!
      ASR      %1           ; GET RID OF READY AND CYCLE BECAUSE OF MAINT MODE
      CMPB    FNCCNT, %1    ; MOVE IT RIGHT ONE PLACE
      BEQ      .+4         ; CHECK AGAINST FNCCNT
      HLT                ; SHOULD BE EQUAL
      INC      FNCCNT       ; FUNCTION BITS DIDN'T INCREMENT IN MAINT MODE
      CMP      #10, FNCCNT  ; GET READY FOR NEXT PASS
      BEQ      MFCHK        ; ONLY 10 BECAUSE FNCT3-1 GO TO ZERO
      MFCHK                ; IF ITS EQUAL GO CHECK DATA

```



```

172340          CHECK:  MOV  INBUF,%2
172341          CHECK:  MOV  INBUF,%3
172342          CHECK:  CLR  LENCHK
172343          CHECK:  INC  LENCHK
172344          CHECK:  CMP  (%2),(%3)+
172345          CHECK:  BEQ  HLT
172346          CHECK:  HLT
172347          CHECK:  CMP  LENCHK,BUFLEN
172348          CHECK:  BNE  COMPRA
172349          CHECK:  MOV  %DRVS,%DRINV
172350          CHECK:  CLR  %DRVS
172351          CHECK:  MOV  %B40,%PSW
172352          CHECK:  RTS
172353          CHECK:  MOV  %52525,%2
172354          CHECK:  MOV  INBUF,%3
172355          CHECK:  CLR  LENCHK
172356          CHECK:  INC  LENCHK
172357          CHECK:  CMP  (%2),(%3)+
172358          CHECK:  BEQ  HLT
172359          CHECK:  HLT

```

```

: IS INBUF FILLED?
: LOAD NEXT BUFFER WORD
: CONTINUE CHECKING
: EXIT
: STARTING ADDRESS OF CHECK-BUFFER TO R2
: CLEAR LENGTH CHECK
: CLEAR R3
: MOVE R3 TO CHKBUF ADDRESS AND INC BY 2
: MOVE R3 TO NEXT CHKBUF ADDRESS AND INC BY 2
: ADD 2 TO LENGTH CHECK
: CHECK FOR DONE
: IS CHECK-BUFFER FILLED?
: NEXT NUMBER FOR BUFFER
: CONTINUE FILLING
: EXIT
: CLEAR IE
: CHECKING FOR ERROR
: ERROR SET?
: ERROR BIT IS SET
: CHECKING READY BIT
: IS READY SET
: FALSE INTERRUPT - ERROR AND READY ARE CLEAR
: TEST1 FOR DRVC=0
: WAS IT EQUAL?
: DRVC NOT =0
: BUFFER LENGTH TO R2
: NUMBER OF TRANSFERS * TIMES 2
: CORRECT DRBA
: CHECKING DRBA
: IS DRBA CORRECT?
: DRBA NOT CORRECT
: RETURN ADDRESS TO RETURN ADDRESS +2
: EXIT
: STARTING ADDRESS OF CHECK BUFFER TO R2
: STARTING ADDRESS OF IN BUFFER TO R3
: CLEAR LENGTH CHECK
: MAKE A COMPARISON
: IS THE DATA CORRECT?
: BRANCH IF OK
: BAD DATA
: SEE IF THE BUFFER HAS BEEN CHECKED
: BUFFER CHECKED?
: RESTORE DR11-8 INTERRUPT VECTOR
: RESTORE DR11-8 INTERRUPT STATUS
: RESTORE PROC TO PRIORITY LEVEL 7
: EXIT
: DATO NUMBER TO R2
: STARTING ADDRESS OF IN BUFFER TO R3
: CLEAR LENGTH CHECK
: MAKE A COMPARISON
: IS THE DATA CORRECT?
: BRANCH IF OK
: BAD DATA

```

Vertical text on the left side of the page, likely a list of addresses or identifiers.

Addresses and labels for various code blocks, such as 172060, 172054, 000100, 172012, 171776, 000207, 177566, 002365, 003407, 004767, 010000, 000104, 000076, 170706, 000072, 170702, 000020, 171672, 007133, 016767, 170660, 000044, 007136, 016767, 170654, 000040, 007144, 012767, 007206, 170642, 007145, 005067, 170640, 007146, 005077, 171632, 007147, 005167, 177740, 007148, 100403, 007170, 052777, 000020, 171616, 007176, 000167, 171754, 007202, 000000, 007204, 000000, 007206, 000002, 007208, 000000.

Assembly code instructions and labels. Includes: LENCHK, BUFLN; COMPRA; ERRCHK; BIT6, DRST; DRST; DRST; TRTRAP; TRAP; TRPB; YESTR; YESTR2; YESRT; HALT.

Comments and control flow instructions. Includes: :SEE IF THE BUFFER HAS BEEN CHECKED; :BUFFER CHECKED?; :CHECK END OF BUFFER + 1; :SEE IF TOO MANY WORDS WERE TRANSFERRED; :TOO MANY; :EXIT; :CLEAR IE; :CHECKING FOR ERROR; :ERROR SET?; :ERROR BIT IS SET; :CHECKING READY BIT; :IS ROY SET; :FALSE ENTRY - ERROR AND READY ARE CLEAR; :EXIT; :*****; :BELL ON PASS COMPLETE; :*****; :ROUTINE TO CHECK FOR TRACE TRAP TO BE RUN WITH PROGRAM; :*****; :CHECK FO CONT G; :SHOULD WE RUN WITH TRACE TRAP; :YES; :NO HAVE WE RAN WITH TRACE TRAP ON; :IF SO RESTORE PREVIOUS CONTENTS; :CLEAR TRACE TRAP; :START OF TEST WITH TRACE OFF; :*****; :SAVE OLD CONTENTS. SET UP FOR TRACE TRAP; :*****; :SAVE ODT PC; :SAVE ODT STATUS; :NEW TRAP VECTOR; :NEW CONDITION CODES; :SET TRACE TRAP; :START OF TEST WITH TRACE ON; :STORAGE FOR ODT PC; :STORAG FOR ODT STATUS; :RETURN TO PROGRAM FROM TRAP; :RTI FAILED.


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```
::*****  
: SLAVE START  
:*****
```

```
SSI:   NOP  
       MOV      #BUFF,R6  
       JSR      RT,SETVEC      ;SET UP INTERRUPT VECTORS  
       CLR      JBFLAG  
       MOV      #SJOB1,NEXJOB ;FOR READY INTERRUPT  
       MOV      #SJOB2,NEXJOB+2 ;FOR ERROR INTERRUPT  
       MOV      #34,C,PSW      ;RAISE CP PRIORITY TO 7  
       MOV      #TE,CORST      ;SET INTERRUPT ENABLE  
       CLR      PSW           ;DROP CP PRIORITY TO 0 AND ENTER BACKGROUND
```

```
::*****  
: BACKGROUND PROGRAM; WAITS FOR JBFLAG TO SET  
:*****
```

```
BACKGD: INC      R0  
        INC      R1  
        INC      R2  
        INC      R3  
        INC      R4  
        INC      R5  
        COMP     R0,R5  
        BEQ     .+6  
        HALT  
        HALT     ;BACKGROUND TEST FAILED  
        CMP     R1,R4  
        BEQ     .+6  
        HALT  
        HALT     ;BACKGROUND TEST FAILED  
        CMP     R2,R3  
        BEQ     .+6  
        HALT  
        HALT     ;BACKGROUND TEST FAILED  
        TST     JBFLAG  
        BEQ     BACKGD ;ANY JOBS?  
        BRN     .+6     ;BRANCH IF NONE  
        JSR     R5,SAVALL ;YES & EXECUTE JOB WHOSE ADDRESS IS IN JBFLAG  
        CLR     NEXJOB  
        CLR     NEXJOB+2  
        MOV     JBFLAG,34  
        CLR     JBFLAG  
        TRAP  
        TRAP     ;TRAP THROUGH JBFLAG AT 34  
        JSR     R5,RESALL  
        BR     BACKGD
```

```
::*****  
: SUBROUTINE TO PUSH ALL REGISTERS ONTO THE STACK  
:*****
```

```
SAVALL: MOV     R4,-(R6)  ;R5 WAS PUSHED BY JSR  
        MOV     R3,-(R6)  
        MOV     R2,-(R6)
```

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1761 007474 010146
1762 007476 010046
1763 007500 000115
1764 007520 005767
1765 007524 001402
1766 007530 104000
1767 007534 000000
1768 007538 004000 171202
1769 007542 001411
1770 007546 005767 177370
1771 007550 001002
1772 007554 104000
1773 007558 000000
1774 007562 016767 177356 177356
1775 007564 000002
1776 007566 005002
1777 007570 005003
1778 007574 005004
1779 007578 005005
1780 007582 000207
1781 007586 171306
1782 007590 007600
1783 007594 171274
1784 007598 011072 170256
1785 007602 016767 170262
1786 007606 005067 170260
1787 007610 016767 171250 170254
1788 007614 005000
1789 007618 005001
1790 007622 005002
1791 007626 005003
1792 007630 005004
1793 007634 005005
1794 007638 000207

```

```

MOV R1, -(R6)
MOV R0, -(R6)
JMP (R5) ;R5 HOLDS RETURN ADDRESS

:*****
: SUBROUTINE TO POP ALL REGISTERS OFF THE STACK
:*****

RESALL: TST (R6)+
MOV (R6)+, R0
MOV (R6)+, R1
MOV (R6)+, R2
MOV (R6)+, R3
MOV (R6)+, R4
RTS R5

:*****
: ROUTINE TO SET UP INTERRUPT VECTORS
:*****

SETVEC: MOV DRINV, R0 ;R0 IS VECTOR ADDRESS
MOV #DRINS, (R0)+ ;PUT SERVICE ADDRESS INTO VECTOR
MOV DRINL, (R0) ;PUT PRIORITY INTO VECTOR+2
MOV #PRINT, R0 ;SET UP EMT ADDRESS
MOV DRINL, R2 ;SET UP EMT PRIORITY LEVEL
CLR R3
MOV DRINL, R6 ;SET UP TRAP ADDRESS
CLR R0 ;INITIALIZE REGISTERS
CLR R1
CLR R2
CLR R3
CLR R4
CLR R5
RTS R7

:*****
: PRIMARY INTERRUPT SERVICE ROUTINE.
: SETS UP JBLFLAG WITH ADDRESS OF JOB TO BE RUNSTARS
:*****

DRINS: TST JBLFLAG ;HAS THE PREVIOUS INTERRUPT BEEN SERVICED?
BEQ DRINO
HLT
HALT ;NO
DRINC: BIT #DSTATC, DRST ;CHECK FOR ERROR
BEQ DRIN3 ;BRANCH IF NO ERROR
TST NEXJOB+2 ;IS THERE AN ERROR SERVICE ROUTINE?
BNE DRIN1 ;BRANCH IF THERE IS.
HLT ;ERROR INTERRUPT, NO ERROR SERVICE.
DRIN1: MOV NEXJOB+2, JBLFLAG ;SET UP JOBFLAG WITH ADDRESS OF SERVICE ROUTINE
RTI
DRIN3: TSTB DRST ;CHECK READY
BMI DRIN2 ;BRANCH IF SET
HLT
DRIN2: TST NEXJOB ;INTERRUPT WITHOUT ERROR OR READY
;IS THERE A READY SERVICE ROUTINE

```

```

007662 001002 BNE .+6 ;BRANCH IF THERE IS.
007664 104000 HLT
007666 000000 HLT
007668 177320 177322 MOV NEXJOB,JBFLAG ;READY INTERRUPT, NO READY SERVICE
007670 000002 RTI ;SET UP JOBFLAG WITH SERVICE ROUTINE ADDRESS

```

```

*****
ROUTINE A, SEGMENT 0
FILL BUFFER AND TRANSMIT
*****

```

```

007700 012700 011034 JOBAD: MOV #LISTA,R0 ;R0 IS XMIT LIST ADDRESS
007704 012701 011046 MOV #LISTA1,R1 ;LISTA1 WILL BE REC LIST
007710 012021 MOV (R0)+,(R1)+ ;START WITH BUS ADDRESSES EQUAL
007712 012002 MOV (R0)+,R2 ;R2 HOLDS WORD COUNT OF XMIT
007714 010211 MOV R2,(R1) ;MAKE REC WORD COUNT THE SAME
007716 005402 NEG R2 ;MAKE WORD COUNT POSITIVE
007720 006302 ASL R2 ;TRANSFORM INTO BYTE COUNT
007722 060241 ADD R2,-(R1) ;ADD TO REC BUS ADDRESS
007724 005010 CLR (R0) ;CLEAR OFFSET IN XMIT LIST
007726 024040 CMP -(R0),-(R0) ;LEAVE R0=LISTA=XMIT LIST

```

```

007730 022767 000100 177264 CMP #100,JBONT ;ENOUGH PASSES FOR BELL?
007736 003010 BGT JOBADA ;BRANCH IF NOT ENOUGH
007740 105737 177564 JOBACB: TSTB @#177564 ;TTY READY?
007744 100375 BPL JOBACB
007746 012737 000207 177556 MOV #207,@#177566 ;RING BELL
007754 005067 177242 CLR JBONT ;RESET JOB COUNT
007760 004767 000704 JOBADA: JSR R7,SETBUF ;FILL UP XMIT BUFFER WITH SPECIAL BINARY COUNT
007764 012700 011034 MOV #LISTA,R0
007770 004767 000370 JSR R7,XMIT ;TRANSMIT DATA TO SLAVE
007774 012767 010012 177212 MOV #JOB1,NEXJOB ;JOB1 IS NEXT
010002 012767 000000 177206 MOV #0,NEXJOB+2 ;NO ERROR RECOVERY
010010 000002 RTI ;RETURN TO BACKGROUND VIA TRAP

```

```

*****
ROUTINE A, SEGMENT 1
FLUSH A BUFFER AND RECEIVE DATA
*****

```

```

010012 012700 011046 JOB1: MOV #LISTA1,R0 ;PUT REC LIST ADDRESS INTO R0
010016 004767 000574 JSR R7,FLUSH ;FLUSH BUFFER
010020 012700 011046 MOV #LISTA1,R0
010024 004767 000406 JSR R7,MREC ;RECEIVE DATA FROM SLAVE
010032 012767 010050 177154 MOV #JOB2,NEXJOB ;JOB2 IS NEXT
010040 012767 000000 177150 MOV #0,NEXJOB+2 ;NO ERROR RECOVERY
010046 000002 RTI

```

```

*****
ROUTINE A, SEGMENT 2
CHECKS TRANSMITTED DATA WITH RECEIVED
*****

```

```

010050 012700 011034 JOB2: MOV #LISTA,R0 ;XMIT BUFFER LIST
010054 012701 011046 MOV #LISTA1,R1 ;REC BUFFER LIST
010060 004767 000642 JSR R7,BUFCHK ;COMPARE THE TWO BUFFERS

```

```

18934 010064 042777 000100 170730
18935 010072 012777 000100 170722
18936 010100 012767 000100 177106
18937 010106 012767 000000 177102
18938 010114 035267 177102
18939 010120 000002

```

```

BIC #IE,DRST ;GLITCH INTERRUPT
MOV #IE,DRST
MOV #JOBAD,NEXJOB ;REPEAT JOBAD
MOV #0,NEXJOB+2
INC JBCNT ;ADVANCE COUNT
RTI

```

```

;*****
; SLAVE'S INTERRUPT SERVICE ROUTINES
;*****

```

```

JOB1: IGNORE FIRST READY INTERRUPT
;*****

```

```

18947 010122 012767 000000 177064
18948 010130 012767 010140 177060
18949 010136 000002

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SJOB1: MOV #0,NEXJOB ;NO MORE READY INTERRUPTS
MOV #SJOB2,NEXJOB+2 ;UNTIL ATTN INTERRUPT
RTI

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;*****
; JOB2: WAIT FOR COMMAND
;*****

```

```

18955 010140 032777 004000 170654
18956 010146 001002
18957 010150 104000
18958 010152 000000
18959 010154 005001
18960 010156 016702 170640
18961 010162 012703 000010
18962 010166 012704 004000
18963 010172 016705 170626
18964 010176 012700 011062
18965 010202 004767 000122
18966 010206 012700 011060
18967 010212 016010 000004
18968 010216 066710 170516
18969 010222 012077 170572
18970 010226 012077 170564
18971 010232 005077 170564
18972 010236 032777 002000 170556
18973 010244 001405
18974 010246 032777 000400 170546
18975 010254 001774
18976 010256 000412
18977 010260 012700 011060
18978 010264 004767 000356
18979 010270 052777 000004 170524
18980 010276 042777 000400 170516
18981 010304 052777 000101 170510
18982 010312 012767 010122 176674
18983 010320 012767 010140 176670
18984 010326 000002

```

```

SJOB2: BIT #DSTATC,DRST ;TEST FOR INTER
BNE SJOB2A
HLT
SJOB2A: CLR R1 ;ERROR OTHER THAN DSTATC
MOV DRST,R2 ;SET UP FOR PARAMETERS
MOV #FNCT3,R3 ;R2 IS STATUS ADDRESS
MOV #DSTATC,R4 ;R3 IS FUNCTION BIT 3
MOV DRDB,R5 ;R4 IS INTERRUPT BIT
MOV #LISTB+2,R0 ;R5 IS DATA BUFFER ADDRESS
JSR R7,HNDCHK ;STORE PARAMETERS HERE STARTING WITH WORD COUNT
MOV #LISTB,R0 ;GET PARAMETERS
MOV 4(R0),(R0) ;R0 IS TOP OF LIST
ADD INBUF,(R0) ;MOVE OFFSET TO TOP
MOV (R0)+,DRBA ;TOP OF LIST IS BUFFER START + OFFSET
MOV (R0)+,DRWC ;SET UP BUS ADDRESS
CLR DRST ;SET UP WORD COUNT
BIT #DSTATB,DRST ;CLEAR ALL FUNCTION BITS
BEQ SJOB2C ;WHICH DIRECTION
BIT #CYCLE,DRST ;BRANCH IF RECIEVE (LEAVE FNCT1 CLEAR FOR DATI'S)
BEQ SJOB2B ;WAIT FOR MASTER TO SET CYCLE
BR SJOB2D ;BRANCH IF NOT SET
MOV #LISTB,R0 ;GO DO THE COMAND
JSR R7,BLUSH ;BLUSH THE BUFFER
BIS #FNCT2,DRST ;SET FNCT2 FOR DATO'S
BIC #CYCLE,DRST ;CLEAR CYCLE
SJOB2C: BIS #IE!GO,DRST ;EXECUTE COMMAND AND INTERRUPT WHEN DONE
MOV #SJOB1,NEXJOB ;IGNORE READY INTERRUPT
MOV #SJOB2,NEXJOB+2 ;WAIT FOR ATTN INTERRUPT
RTI

```

```

;*****
; SLAVE ROUTINE TO ACCEPT PARAMETERS FROM MASTER
;*****

```

```

1940 010514 052777 000101 170300
1941 010522 000207
1942
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1944
1945
1939 010506 052777 000400 170306
1938 010504 001374
1937 010476 032777 002000 170316
1936 010472 004767 000026
1935 010454 012777 000004 170330
1934 010462 000000
1933 010460 104000
1932 010456 100402
1931 010452 105777 170344
1930 010450 000000
1929 010446 104000
1928 010444 100002
1927 010440 005777 170356
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1920 010430 052777 000101 170364
1919 010422 042777 000400 170372
1918 010416 004767 000102
1917 010410 012777 000000 170404
1916 010406 000000
1915 010404 104000
1914 010402 100402
1913 010376 105777 170420
1912 010374 000000
1911 010370 104000
1910 010364 005777 170432
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```

MNDSH:  MOV (R5), (R5) ; ECHO PARAMETER
        MOV (R5), (R0)+ ; STORE PARAMETER
        BIS R3, (R2) ; REPLY WITH FNCT3
MNDSH1: BIT R4, (R2) ; WAIT FOR ATTN TO DROP
        BNE MNDSH1
        BIC R3, (R2) ; DROP FNCT3
        INC R1 ; CHECK NUMBER
        CMP R1, NWRDXF
        BLT MNDSH2 ; BRANCH IF NOT DONE YET
MNDSH2: BIT R7
        BEQ MNDSH2 ; BRANCH IF ATTN CLEAR
        BR MNDSHK ; GET ANOTHER PARAMETER

```

```

;*****
; MASTER TRANSMIT ROUTINE
; ENTER WITH TRANSFER LIST IN R0
;*****

```

```

MXMIT:  TST @DRST ; MAKE SURE ERROR IS CLEAR
        BPL MXMIT1 ; AND READY IS SET
        HLT ; ERROR IS SET
MXMIT1: TSTB @DRST
        BMI MXMIT2
        HLT
MXMIT2: MOV #0, @DRST ; READY NOT SET
        JSR R7, PRMXFR ; SET UP FUNCTION FOR DATI'S
        BIC #CYCLE, @DRST ; TRANSFER PARAMETERS OF LIST WHOSE ADDRESS IS IN R0
        BIS #IE!GO, @DRST ; MAKE SURE CYCLE IS CLEAR
        RTS R7 ; EXECUTE COMMAND AND INTERRUPT WHEN DONE

```

```

;*****
; MASTER RECEIVE ROUTINE
; ENTER WITH TRANSFER LIST IN R0
;*****

```

```

MREC:   TST @DRST ; MAKE SURE ERROR IS CLEAR
        BPL MREC1 ; AND READY SET.
        HLT ; ERROR SET
MREC1:  TSTB @DRST
        BMI MREC2
        HLT
MREC2:  MOV #FNCT2, @DRST ; READY CLEAR
        JSR R7, PRMXFR ; SET UP FUNCTION FOR DATO'S
        BIT @DSTATB, @DRST ; TRANSFER PARAMETERS OF LIST WHOSE ADDRESS IS IN R0
        BNE MREC3 ; WAIT FOR SLAVE TO CLEAR DIRECTION
        BIC #CYCLE, @DRST ; BRANCH IF SET
        BIS #IE!GO, @DRST ; CLEAR CYCLE
        RTS R7 ; EXECUTE COMMAND AND INTERRUPT WHEN DONE.

```

```

;*****
; ROUTINE TO TRANSFER AND CHECK PARAMETERS UNDER FLAG CONTROL
; ENTER WITH R0 POINTING TO TRANSFER LIST
;*****

```


K03

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2278.P1:

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```

1946
1947
1948 010524 012077 170270 PRMXFR: MOV (R0)+,DRBA ;FIRST WORD IN LIST IS ADDRESS
1949 010530 011077 170262 MOV (R0),DRWC ;SECOND WORD IN LIST IS WORD COUNT
1950 010534 005001 CLR R1 ;R1 COUNTS PARAMETERS TRANSFERRED
1951 010536 016702 170260 MOV DRST,R2 ;R2 IS THE STATUS ADDRESS
1952 010542 012703 000010 MOV #FNCT3,R3 ;R3 USED FOR FUNCTION BIT 3
1953 010546 012704 004000 MOV #DSTATC,R4 ;R4 USED FOR INTERRUPT BIT
1954 010552 016705 170246 MOV DRDB,R5 ;R5 IS THE DATA BUFFER ADDRESS
1955 010556 011015 PRMXF1: MOV (R0),(R5) ;SET UP DRDB WITH PARAMETER
1956 010560 050312 BIS R3,(R2) ;CALL SLAVE'S ATTN
1957 010562 030412 PRMXF2: BIT R4,(R2) ;WAIT FOR REPLY
1958 010564 001776 SEQ PRMXF2 ;BRANCH IF ATTN CLEAR
1959 010566 022015 CMP (R0)+,(R5) ;COMPARE PARAMETER SENT WITH SLAVE'S ECHO
1960 010570 001402 BEQ PRMXF3 ;BRANCH IF EQUAL
1961 010572 104000 HLT ;PARAMETER DID NOT ECHO
1962 010574 000000 HALT ;DROP SLAVE'S ATTN
1963 010576 040312 PRMXF3: BIC R3,(R2) ;WAIT FOR REPLY
1964 010600 030412 PRMXF4: BIT R4,(R2) ;BRANCH IF ATTN SET
1965 010602 001376 BNE PRMXF4 ;ADVANCE PARAMETER COUNT
1966 010604 005201 INC R1 ;ALL PARAMETER XFERRED?
1967 010606 020167 176400 CMP R1,NURDXF ;BRANCH IF NOT DONE
1968 010612 002761 BLT PRMXF1 ;RETURN WHEN ALL PARAMETERS TRANSFERRED AND CHECKED.
1969 010614 000207 RTS R7
1970
1971
1972
1973
1974
1975
1976 010616 005005 FLUSH: CLR R5 ;SET R5 TO ZIP
1977 010620 004767 000030 JSR R7,BSETUP ;SET UP REGISTERS
1978 010624 004767 000004 FLUSH1: JSR R7,BUFPUT ;STORE ITEM IN BUFFER
1979 010630 002775 BLT FLUSH1
1980 010632 000432 BR BUFOUT ;STOP WHEN BUFFER FULL
1981
1982 010634 010521 BUFPJT: MOV R5,(R1)+ ;PUT R5 INTO BUFFER
1983 010636 060503 ADD R5,R3 ;INCLUDE IN CHECKSUM
1984 010640 005504 ADC R4
1985 010642 005202 INC R2 ;ADVANCE WORD COUNT
1986 010644 000207 RTS R7 ;RETURN WITH STATUS SET
1987
1988
1989
1990
1991
1992 010646 012705 177777 BLUSH: MOV #-1,R5 ;SET R5 TO ALL ONE'S
1993 010652 000762 BR FLUSH+2
1994
1995
1996 010654 012001 ;REGISTER SETUP ROUTINE
1997 010656 012002 BSETUP: MOV (R0)+,R1 ;R1 IS BUS ADDRESS
1998 010660 005720 MOV (R0)+,R2 ;R2 IS WORD COUNT
1999 010662 005003 TST (R0)+ ;SKIP OVER OFFSET
2000 010664 005004 CLR R3 ;CLEAR LOW CHECKSUM
2001 010666 000207 CLR R4 ;CLEAR HIGH CHECKSUM
RTS R7 ;RETURN

```



```

2058 011016 000207
2059 011020 104000
2060 011022 012105
2061 011024 060503
2062 011026 005504
2063 011030 005202
2064 011032 000207
2065 011034 013570
2066 011036 177605
2067 011040 000000
2068 011042 000000
2069 011044 000000
2070 011046 000000
2071 011050 000000
2072 011052 000000
2073 011054 000000
2074 011056 000000
2075 011060 013570
2076 011062 000000
2077 011064 000000
2078 011066 000000
2079 011070 000000
2080 011072 004767 000654
2081 011076 037727 167710 020000
2082 011104 001401
2083 011106 000002
2084 011110 012667 000172
2085 011114 012667 000170
2086 011120 024646
2087 011122 012777 000215 167734
2088 011130 105777 167726
2089 011134 100375
2090 011136 012777 000212 167720
2091 011144 105777 167712
2092 011150 100375
2093 011152 010267 000122
2094 011156 010367 000120
2095 011162 010467 000116
2096 011166 016702 000114
2097 011172 004767 000114
2098 011176 012777 000240 167660
2099 011204 105777 167652
2100 011210 100375
2101 011212 016702 000072

```

```

      RTS      R7      ;RETURN IF CHECKSUM OK.
CHKSM2: HLT
      GETBUF: MOV     (R1)+,R5 ;GET ITEM OUT OF BUFFER
      ADD     R5,R3      ;ADD TO CHECKSUM
      ADC     R4
      INC     R2
      RTS      R7      ;ADVANCE WORD COUNT

LISTA: XINBUF          ;START OF XMIT BUFFER
      -123.           ;WORD COUNT
      0              ;OFFSET
      0              ;CHECKSUM LOW
      0              ;CHECKSUM HIGH

LISTA1: 0              ;START OF REC BUFFER
      0              ;WORD COUNT
      0              ;OFFSET
      0              ;CHECKSUM LOW
      0              ;CHECKSUM HIGH

LISTB: XINBUF          ;SLAVE'S ECHO BUFFER
      0
      0
      0
      0

;*****
;      ENTERED WITH SYSTEM TRAP CALL(HLT)
;      PRINT OUT THE ERROR PC AND STATUS REGISTER
;*****

PRINT: JSR      %7,CKSWR
      BIT      @SR,#20000 ;TEST FOR INHIBIT PRINT ON
      BEQ     .+4         ;BRANCH TO PRINT
      RTI      ;INHIBIT, RETURN TO MAIN STREAM
      MOV     (6)+,SAVPC  ;PC OF FAILING ROUTINE
      MOV     (6)+,SAVCC  ;CC OF ERROR CONDITION
      CMP     -(6),-(6)   ;REPOSITION THE STACK
      MOV     #215,@TPB  ;CR
      TSTB   @TPS
      BPL    .-4
      MOV     #212,@TPB  ;LINE FEED
      TSTB   @TPS
      BPL    .-4
      MOV     %2,SAVR2   ;SAVE R2
      MOV     %3,SAVR3   ;SAVE R3
      MOV     %4,SAVR4   ;SAVE R4
      MOV     SAVPC,%2
      JSR     %7,PRTAB   ;PRINT OCTAL NUMBER
      MOV     #240,@TPB
      TSTB   @TPS
      BPL    .-4
      MOV     SAVCC,%2

```

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011114 011216 004767 000070 JSR %7.PRTAB ;PRINT OCTAL NUMBER
011115 011222 012777 000240 MOV #240,2TPB ;PRINT SPACE
011116 011230 105777 167626 TSTB 2TPS ;PRINTER DONE
011117 011234 100375 BPL -4 ;BRANCH WHEN NOT DONE
011118 011236 017702 167560 MOV 2DRST,%2 ;GET DR118 STATUS
011119 011242 004767 000044 JSR %7.PRTAB ;PRINT OCTAL NUMBER
011120 011246 016702 000026 MOV SAVR2,%2
011121 011252 016703 000024 MOV SAVR3,%3
011122 011256 016704 000022 MOV SAVR4,%4
011123 011262 004767 000464 JSR %7.CKSWR
011124 011266 005777 167520 TST 2SR ;CHECK SR FOR HALT SWITCH
011125 011272 100001 BPL +4
011126 011274 000000 HALT ;HALT ON ERROR UP
011127 011276 000002 RTI ;RETURN TO MAINLINE
011128 011300 000000
011129 011302 000000 SAVR2: 0
011130 011304 000000 SAVR3: 0
011131 011306 000000 SAVR4: 0
011132 011310 000000 SAVPC: 0
011133 011312 000000 SAVCC: 0
011134 011314 000000
011135 011316 000000
011136 011318 000000
011137 011320 000000
011138 011322 000000
011139 011324 000000
011140 011326 000000
011141 011328 000000
011142 011330 000000
011143 011332 000000
011144 011334 000000
011145 011336 000000
011146 011338 000000
011147 011340 000000
011148 011342 000000
011149 011344 000000
011150 011346 000000
011151 011348 000000
011152 011350 000000
011153 011352 000000
011154 011354 000000
011155 011356 000000
011156 011358 000000
011157 011360 000000
011158 011362 000000
011159 011364 000000
011160 011366 000000
011161 011368 000000
011162 011370 000260 167466 BMI MINUS ;NEG SIGN PRINT 1
011163 011372 000403 167456 BR START ;POS SIGN PRINT 0
011164 011374 012777 000261 MINUS: MOV #261,2TPB
011165 011376 016703 000156 START: MOV SEVEN,%3 ;PUT MASK IN R3
011166 011378 005167 000144 MOV %2,TOODLE ;GET READY TO DOODLE NUMBER IN TOODLE
011167 011380 046703 000140 COM TOODLE ;COMPENSATES FOR COMPLEMENT DURING BIC
011168 011382 001410 BEQ WRTCC ;AND IN OCTAL CHARACTER
011169 011384 066767 000136 MKNUM: WRTCC ;ZERO, WRITE 0 IN LIST
011170 011386 005267 000134 INC DECML,WGTCT ;COUNT UP TO
011171 011388 026703 000126 CMP BINCT,%3 ;AND RECORD
011172 011390 001370 BNE MKNUM ;SAME BINARY WEIGHT
011173 011392 062767 000260 000120 WRTCC: ADD #260,BINCT ;KEEP COUNTN
011174 011394 016724 000114 MOV BINCT,(4)+ ;ADD ASCII PREFIX
011175 011396 066767 000102 000102 ADD SEVEN,DECML ;WRITE ASCII CHAR IN LIST
011176 011398 005067 000100 CLR WGTCT ;EXPAND BINARY WEIGHT
011177 011400 005067 000076 CLR BINCT
011178 011402 005367 000074 DEC ASCNT
011179 011404 001410 BEQ XLIST ;5 CHAR IN LIST
011180 011406 012703 000003 MOV #3,%3 ;SET X3 FOR ADD LOOP
011181 011408 066767 000052 000050 MCADD: ADD SEVEN,SEVEN ;MAKING SEVENTY BY SEVEN
011182 011410 005303 DEC %3
011183 011412 001373 BNE MOADD
011184 011414 000730 BR START ;NY SEVEN SET GET NY OCTAL
011185 011416 012767 000005 000044 XLIST: MOV #5,ASCNT ;SEND 5 CHAR TO TTY

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000100 166360 15: BIC 0100,2TP5
: CLEAR POINTER TO CHARACTER
: RETURN
: OR, P CHAR?
000137 .EMPTY: CMPB 0,2)
: CHECK FOR RETURN TERMINATOR
000041 CMPB 0,2)
: TYPE CHARACTER
166334 15: YSTB 0105
: SET UP NEW POINTER
166330 .RET: INC %2
: RETR,%2
000020 MOV 0,RET-6
: SAV,%2
012560 BR MOV 0,RET-6
: SAV,%2
000006 .REST: MOV 0,RET-2
: SAV,%2
BR ITOUT

012560 012 041 .RETR: .BYTE 15,12,?!
: EVEN
: SAV: 0
: =,+1000
: FOR STACK POINTER 100 LOCATIONS
BUFF: 0
XINBUF: : =,+1000
XCHKBU: : .END

```


UNSUB	0111310	2099*	2113	2132*															
UNSUB	0111306	2098*	2108	2131*															
UNSUB	0111300	2105*	2120	2128*															
UNSUB	0111302	2104*	2121	2129*															
UNSUB	0111304	2103*	2122	2130*															
UNSUB	1044000	452*	563*	575*	590	599	613	625	638	655	672	685	699	711					
UNSUB	1044000	724*	737*	750*	809	827	841	854	859	882	900	912	941	952					
UNSUB	1044000	994*	1041	1075	1096	1115	1134	1153	1178	1208	1230	1250	1273	1303					
UNSUB	1044000	1301*	1312	1335	1366	1392	1417	1451	1470	1491									
UNSUB	0111614	2199*	2200*	2211	2218														
UNSUB	0111636	2198*	2209*	2211	2218														
UNSUB	0111650	2197*	2217*	2219*	2223*														
UNSUB	0111732	2215	2217*	2219*	2223*														
UNSUB	0111736	2214	2216	2219*	2223*														
UNSUB	0110676	2010*	2016	2019*	2023*														
UNSUB	0106706	1806*	2009*	2019*	2023*														
UNSUB	0075220	1658	1674	1742*	1742*														
UNSUB	0115770	2139*	2148	2159	2165*	2180*													
UNSUB	0101222	1676	1847*	1822	1833														
UNSUB	0101440	1677	1848	1855*	1833														
UNSUB	0101554	1856	1859*	1855*	1833														
UNSUB	0102246	1874*	1875	1855*	1833														
UNSUB	0102260	1873	1877*	1855*	1833														
UNSUB	0103304	1876	1891*	1855*	1833														
UNSUB	0000006	540*	541*	546	548	549	1626*												
UNSUB	0010106	540*	543	547*	550	1583	2093	2124	2136	2210	2213	2238	2250	2294*					
UNSUB	0010022	513*	513*	547*	550	1583	2093	2124	2136	2210	2213	2238	2250	2294*					
UNSUB	0073304	513	1672*	2146	2148*	2168													
UNSUB	0114306	2146	2148*	2168	2148*	2168													
UNSUB	0010722	503	540*	540*	540*														
UNSUB	0001776	494*	547	550	2238	2238													
UNSUB	0117442	2233*	2254*	2255*	2275*	2277*	2278*	2280*	2284	2284	2271	2279*	2280	2294*	2298*				
UNSUB	0117500	2236*	2242*	2243*	2244	2258*	2259	2252	2269	2269	2271	2279*	2280	2294*	2298*				
UNSUB	0010660	2301	534*	2242	2293*	2298													
UNSUB	0010556	533*	1342*	2240	2292*	2295*	2296												
UNSUB	0035542	1035	1041*	1070	2295*	2295*	2296												
UNSUB	0033306	995*	1037	1070	2295*	2295*	2296												
UNSUB	0115666	2149*	2150*	2151	2179*	2179*													
UNSUB	0010664	536*	2099*	2102*	2110*	2115*	2145*	2147*	2172*	2301*	2347*								
UNSUB	0010662	535*	2100	2103	2111	2116	2137*	2141	2170	2176	2299	2339*	2345						
UNSUB	0071222	1586	1590*	2103	2111	2116	2137*	2141	2170	2176	2299	2339*	2345						
UNSUB	0071226	1591*	1601*	2103	2111	2116	2137*	2141	2170	2176	2299	2339*	2345						
UNSUB	0070556	1582*	1601*	2103	2111	2116	2137*	2141	2170	2176	2299	2339*	2345						
UNSUB	0053220	1324*	1328	2103	2111	2116	2137*	2141	2170	2176	2299	2339*	2345						
UNSUB	0122552	2257	2292*	2103	2111	2116	2137*	2141	2170	2176	2299	2339*	2345						
UNSUB	0122772	2296*	2297	2103	2111	2116	2137*	2141	2170	2176	2299	2339*	2345						
UNSUB	0123306	2299*	2300	2103	2111	2116	2137*	2141	2170	2176	2299	2339*	2345						
UNSUB	0124622	500	502	1576	2247	2249	2253	2265	2274	2334*	2348	2354							
UNSUB	0035334	1022	1036*	2103	2111	2116	2137*	2141	2170	2176	2299	2339*	2345						
UNSUB	003706	1054	1069*	2103	2111	2116	2137*	2141	2170	2176	2299	2339*	2345						
UNSUB	003714	1068	1075*	2103	2111	2116	2137*	2141	2170	2176	2299	2339*	2345						
UNSUB	0113556	2141*	2142	2103	2111	2116	2137*	2141	2170	2176	2299	2339*	2345						
UNSUB	0115334	2170*	2171	2175	2175	2175	2175	2175	2175	2175	2175	2175	2175	2175					
UNSUB	0010552	521*	1079*	1080*	1081	1100*	1101*	1102	1119*	1119*	1120	1138*	1139*	1140					
UNSUB	0010552	1369*	1370*	1371	1396*	1397*	1398	1453*	1454*	1457	1472*	1473*	1476						

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SEP-76

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U.S. DEPARTMENT OF JUSTICE

SEP 10 1976
FBI - MEMPHIS

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CHARGE OF JURY AT 10:15 AM
FEDERAL BUREAU OF INVESTIGATION
U.S. DEPARTMENT OF JUSTICE
MEMPHIS, TENNESSEE
SEP 10 1976

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NO.	SYMBOL	NO.	SYMBOL	NO.	SYMBOL	NO.	SYMBOL	NO.	SYMBOL	NO.	SYMBOL	NO.	SYMBOL	NO.	SYMBOL	NO.	SYMBOL
1360	1442	1527	1510	1524	1525	1529	1796	1568	1982	2052	2153						
2279	667	645	662	679	692	705	719	731	744	779	793						
9900	1000	1004	1009	1015	1020	1031	1057	1060	1059	1030	1095						
1434	1513	1589	1834	1890	1895	1919	1939	1963	2151	2243	2333						
673	686	712	725	739	751	810	813	893	912	922	951						
983	1430	1603	1879	1981	1992	1940	1956										
657	661	674	678	691	700	704	713	717	726	730	739						
885	759	762	765	771	774	778	791	794	797	790	794						
997	1000	904	909	929	943	947	964	950	951	975	979						
1872	1874	1893	1900	1937	1964	2093	2136	2210	2213	1484	1593						
1979	2044	2053	1226	1317	1325	1327	1345	1357	1519	1565	1622	1774					
1200	1216	1219	701	714	727	740	754	757	760	763	769						
658	675	688	890	905	909	925	944	949	949	969	977						
1200	1163	1169	1282	1292	1354	1541	1557	1768	1768	1768	1855						
2144	2057	2155	2167	2197	2211	2214	2245	2260	2260	2263	2267						
658	1321	1503	1515	1574	1574	1803	1910	1928	2101	2104	2112						
2177	2177	2241	2297	2300	2346	2346	2346	2346	2101	2104	2112						
896	896	915	935	1022	1025	1037	1054	1068	1070	1068	1068						
2016	2016	2141	2141	2141	2141	2141	2141	2141	2141	2141	2141						
1050	1050	1050	1050	1050	1050	1050	1050	1050	1050	1050	1050						
1030	1030	1030	1030	1030	1030	1030	1030	1030	1030	1030	1030						
1030	1030	1030	1030	1030	1030	1030	1030	1030	1030	1030	1030						
2166	2173	2261															
1050	1050	1050	1050	1050	1050	1050	1050	1050	1050	1050	1050						

